



V.S.S.U.T., Burla
Letter: 402
04.11.2022
Electronics & Telecom. Engg.

VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY, ODISHA
P.O: Engineering College Burla (Siddhi Vihar), Dist: Sambalpur
Odisha- 768018, India

No. VSSUT/ETC/402/2022

Date: 04.11.2022 (04.11.2022)

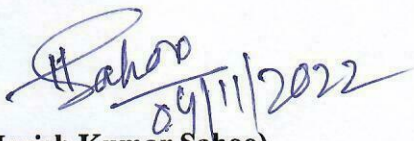
Advertisement for Post of Project Fellow (One position) for State Council on Science & Technology (DST), Govt. of Odisha sponsored project

Applications are invited from eligible students for the position of Project Assistant fellow (one-position) for the State Council on Science & Technology, Odisha, Govt. of Odisha funded project, under the principal investigator Dr. Harish Kumar Sahoo, Professor, Department of Electronics & Telecommunications, Veer Surendra Sai University of Technology, Burla, Sambalpur, Odisha. Interested and eligible candidates are requested to send hard copy of completed application (Annexure -1) along with self-attested copies of supporting documents to the **Registrar, Veer Surendra Sai University of Technology, Burla, Sambalpur-768018**, on or before **20 November, 2022** by speed/registered post/courier. The details of the project are as follows:

Name of the Project	FPGA based Adaptive Power Quality Estimator for Smart Grid Applications
Principal Investigator	Prof. Harish Kumar Sahoo, Dept. of ETC
Co-Principal investigator	Dr. Raseswari Pradhan, Dept. of EE
Qualification	Essential: M.Tech. (with good academic records) in EE/EEE/ETC from a recognized Institute/University Preference will be given for GATE qualified students. Preferable Skill: Applicants having knowledge about MATLAB Programming, Xilinx FPGA, Fourier Analysis, Signal Processing and ML Based Optimization Techniques.
Fellowship	As per revised DST (Govt. of Odisha) Rules. Remuneration for Project Fellow: Rs.17000/- per months for 1st and 2nd year and Rs.19000/- per month for 3rd year.
Nature and duration of post	The work will involve analysis of power quality issues of a system with real time acquisition of power signals, development of advanced signal processing/ ML models for estimation and implementation in Xilinx FPGA. The appointment will be purely temporary basis and will be terminated with completion of the project. The PI and Institute reserves the right to terminate the engagement of the project fellow at any time, if the performance is not found satisfactory. The person engaged shall not be entitled for any claim implicit or explicit for permanent appointment in the University.

General Term and Condition:

1. Interested and eligible candidates are requested to send hard copy of completed application (Annexure -1) along with self-attested copies of supporting documents to the, **Registrar, Veer Surendra Sai University of Technology, Burla, sambalpur-768018, on or before 20 Nov., 2022 by speed/registered post/courier.** University will not be responsible for any postal delay of application. Applications received after the above mentioned date will be treated as cancelled. On the envelope please inscribe "**Application for the post of Project Fellow (DST, Govt. of Odisha)**", **Department of ETC, VSSUT Burla.**
2. Candidates will be short listed for the interview based on the specialization and availability of candidates and other requirements as per the project.
3. The date and time of interview will be informed via email or phone and only short listed candidates will be allowed to attend the interview.
4. Candidates shortlisted for interview should appear in person with originals of certificates (one set of Xerox), and date of birth proof along with any other relevant information (like copies of publications, awards etc.)
5. No travelling or any other allowances is admissible for attending the interview.
6. Candidates will not be considered in absentia.
7. The Principal Investigator of the project reserves the right to fill or not fill the position and also withdraw the notification at any point of time. In case of any conflict, the decision of PI and the university will be final.
8. All legal implications are subjected to local jurisdiction only.


(Prof. Harish Kumar Sahoo)
Principal Investigator

ANNEXURE-1

Application form for the Post of Project Fellow for State Council on Science & Technology (DST), Govt. of Odisha Sponsored Project

Personal Details:

1. Full Name (In capital):
2. Date of Birth (DD/MM/YY) :
3. Category (GEN/SC/ST/OBC)
4. Marital Status (Single/Married)
5. Gender (Male/Female)
6. Nationality
7. Address for Communication
8. Permanent Address
9. Mobile/Phone No.
10. Email:

Affix a recent passport size photo

Details of School/University/Institute Studied (From Matriculation Onward)

Degree	Discipline	University/Institute	Year	%Marks /CGPA	Division
Class X					
Higher Secondary					
B.Tech.					
M.Tech.					
Any other					

Qualifying Examination (GATE/NET/other National level score) if any:

Professional Experiences (Teaching/Research/Industrial) if any:

Name of Organization	Designation	Nature of Work	From	To

M.Tech. Thesis Title:

Seminar/workshop/conference attended (use extra sheet if needed):

Name of Seminar/Conference etc	Paper presented	Organized by

**Research Publications(if any) in Journals, Conferences, Book and Book chapters
(use extra sheet if needed)**

Awards, patents, prizes etc (use extra sheet if needed):

Any other Relevant Information (use extra sheet if needed):

DECLARATION:

I hereby declare that I have carefully read the instructions and particulars mentioned in the application . The entries made in this application form are correct to the best of my knowledge and belief. If selected for admission, I promise to abide by the rules and regulations of the University. I understand the fact that the decision of the University is final in regard to selection of project fellow. The university shall have the rights to expel me from the institute at any point of time after my admission in case any information furnished by me is found to be false. I agree that I shall abide by the decision of the University.

Place:

Date:

Signature of Applicant