ELECTRONICS CIRCUITS

Lecturer Notes

4TH SEM B.TECH (ELECTRICAL ENGINEERING)

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ELECTRONICS CIRCUITS (3-1-0)

MODULE-I

Diode circuit: Load line concept, clipping circuits, comparators, sampling gate, rectifiers, capacitive filters, additional diode circuit.

Transistor: the junction transistor, transistor as an amplifier, transistor construction, the CE configuration, the CB configuration, the CE cut-off and saturation region, common emitter current gain, the common collector configuration, analytical expression for transistor characteristics, the phototransistor.

Transistor at low frequency: Graphical analysis of the CE model, two-port model and hybrid model, transistor hybrid model, the *h*-parameter, analysis of transistor amplifier circuit using *h*-parameter, the emitter follower, miller's theorem and its duality, cascading transistor amplifiers, simplified CE and CC configuration.

MODULE-II (10 Lectures)

Junction FET and its V-I characteristics, FET small signal model, FET biasing, MOSFET, FET as a voltage-variable resistor (VVR), CD amplifier, the hybrid-pi CE transistor model, hybrid-pi conductance and capacitance, validity of hybrid-pi model, variation of hybrid-pi parameters, the CE short-circuit current gain, current gain with resistive load, single stage CE transistor amplifier response, emitter follower at high frequency.

Classification of amplifier, distortion in amplifier, frequency response of amplifier, bode plots, step response of amplifier, band pass of cascade stages, the RC coupled amplifier, high frequency response of two cascaded CE transistor stages.

MODULE-III (10 Lectures)

Classification of amplifier, feedback concept, transfer gain, negative feedback, input-output resistance, method of analysis of a feedback amplifier, voltage- series, voltage-shunt, current-series and current shunt feedback, effect of feedback on bandwidth, double and three pole transfer function with feedback, approximation analysis of multi-pole feedback, voltage-series, voltage-shunt, current- series and current-shunt frequency response, stability, gain and phase margin, compensation, different type of oscillator, frequency stability.

MODULE-IV (10 Lectures)

The basic operational amplifier (OPAMP), differential amplifier and its transfer characteristics, emitter coupled differential amplifier, IC-OPAMP, offset error voltage and current, temperature drift of input offset voltage and current, measurement of OPAMP parameter and its frequency response, different type of OPAMP compensation and its step response. Basic OPAMP application, differential DC amplifier, AC amplifier, analog integrator and differentiator, active filter, resonant band-pass filter, delay equalizer, comparators, sample-hold circuit, AC/DC convertors, logarithmic amplifier, Schmitt trigger, ECL, TTL and 555-timer.

BOOKS:

1. Millma. J. and Halkias .C. Integrated Electronics, TMH, 2007.
2. S. Salivahanan, N. Suresh Kumar and A. Vallavaraj, Electronic Devices and Circuits, 2nd Edition, TMH, 2007.
3. Robert L. Boylestad and Louis Nashelsky, Electronic Devices and Circuit Theory, 9th Edition, Pearson Education / PHI, 2007.

CHAPTER-1
(Lecture-1 & 2)

1.1The Diode as a Circuit Element

Diodes are referred to as non-linear circuit elements because of the diode characteristic curve i.e.

$$i_D=i_s(e^{v_D/\eta V_T}-1) \quad \text{...(1.1)}$$

Where i_s=reverse saturation current in the range of pA for low-power diode.

$V_T=K_BT/q$ is thermal voltage(about 26 mV at room temperature, T = 300 K).

η=ideality factor($1<\eta<2$).

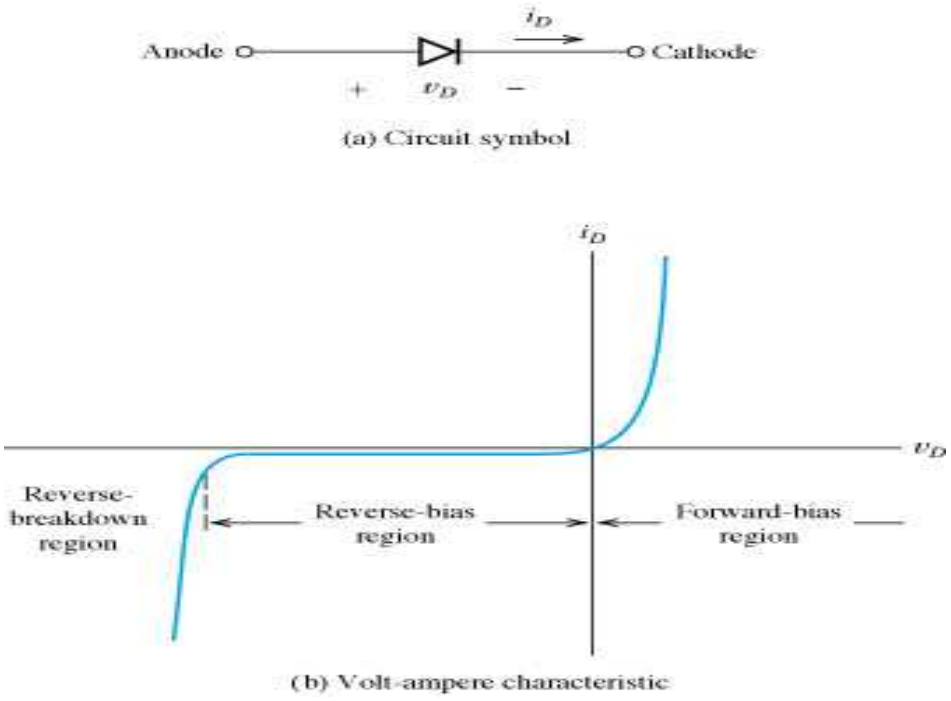


Figure 1.1: a) Circuit symbol for a diode and b) current versus voltage for a semiconductor diode.

For most applications the non-linear region can be avoided and the device can be modeled by piece-wise linear circuit elements. Qualitatively we can just think of an ideal diode has having two regions: a conduction region of zero resistance and an infinite resistance non-conduction region. For many circuit applications, this ideal diode model is an adequate representation of an actual diode and simply requires that the circuit analysis be separated into two parts: forward

current and reverse current. Figure 1.1 shows a schematic symbol for a diode and the current-voltage curve for an ideal diode.

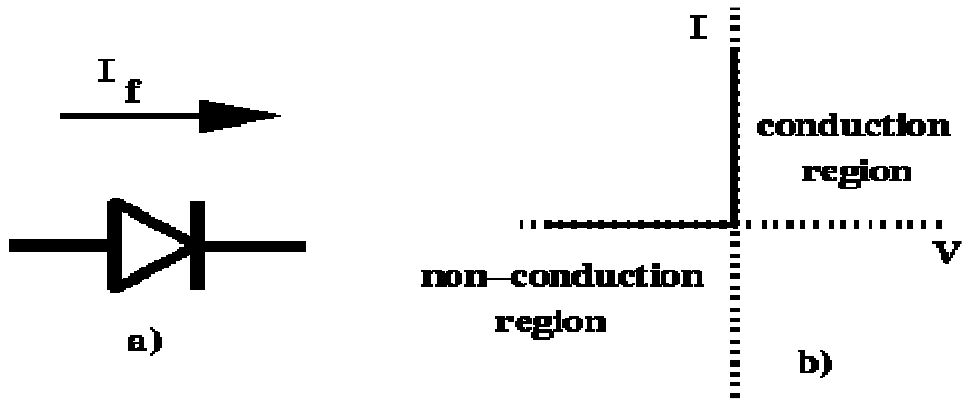


Figure 1.1: a) Schematic symbol for a diode and b) current versus voltage for an ideal diode.

A diode can more accurately be described using the equivalent circuit model shown in figure 1.2. If a diode is forward biased with a high voltage it acts like a resistor (R_f) in series with a voltage source (V_{PN}). For reverse biasing, it acts simply as a resistor (R_r). These approximations are referred to as the linear element model of a diode.

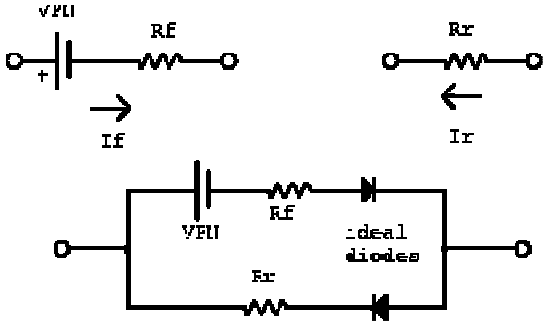
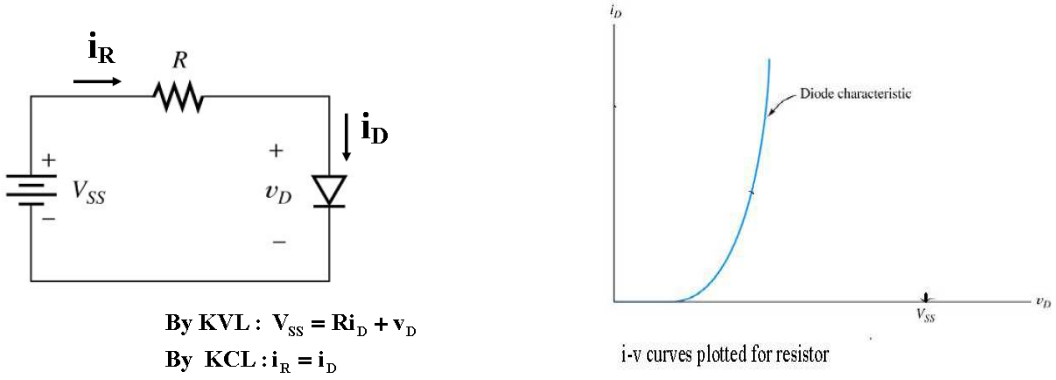


Figure 1.2: Equivalent circuit model of a junction diode.

1.2 Load line concept of Diode:

The applied load will normally have an important impact on the behavior of a device. If the analysis is performed in a graphical manner, a line can be drawn on the characteristics of the device that represents the applied load. The intersection of the load line with the characteristics will determine the point of operation of the system. Such an analysis is called load-line analysis.

Consider the network of Fig. 1.2 using a diode having diode voltageV_D, resistor R and a voltage source V_{ss}. Due to the voltage source a current is established through a series circuit in clock wise manner. The current direction and the defined direction of conduction of the diode is matched so the diode is in the “on” state and conduction has been established.



(a) (b)

Figure 2.1: Series diode configuration (a) circuit (b) characteristics.

Applying Kirchhoff's voltage law to the series circuit of Fig. 2.1 will result in

$$V_{ss}\text{-}Ri_R\text{-}V_D=0$$

$$V_{ss}=Ri_R + V_D \qquad ...(2.1)$$

The intersections of the load line on the characteristics can easily be determined if one simply employs the fact that anywhere on the horizontal axis i_D=0 A and anywhere on the vertical axis V_D= 0 V.

when V_D=0 , then the above equation will be

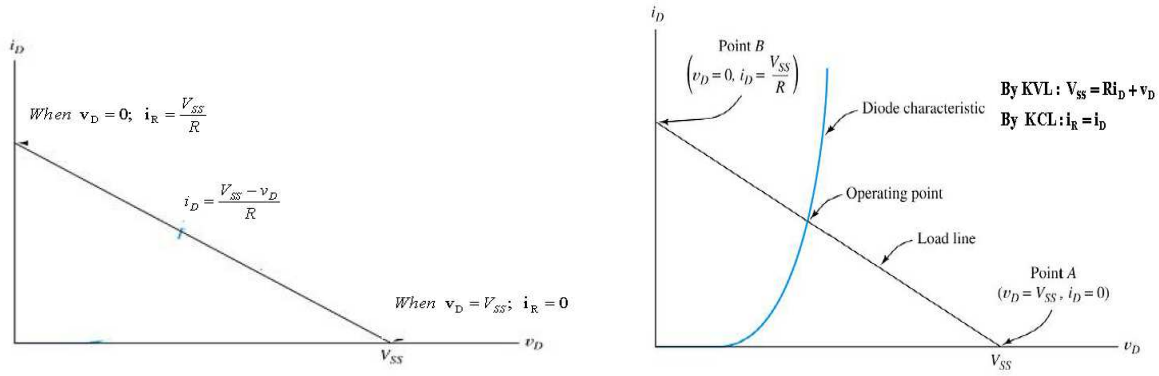
$$V_{ss}=0+Ri_D$$

$$i_D=\left.{}^{V_{ss}}\!/_{R}\right|_{V_D=0} \qquad ...(2.2)$$

Similarly when i_D=0, then the equation 2.1 will be

$$V_{ss}=V_D+ (0\text{A})\, R$$

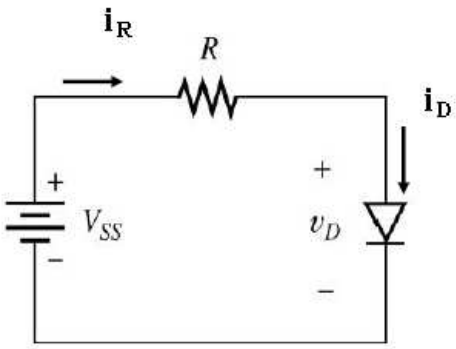
$$V_D=V_{ss}|_{i_D=0} \qquad ...(2.3)$$



(a) (b)

Figure 2.2 :(a)load line graph of the above network (b) intersection of the load line with the characteristics plot

Example on load line analysis:



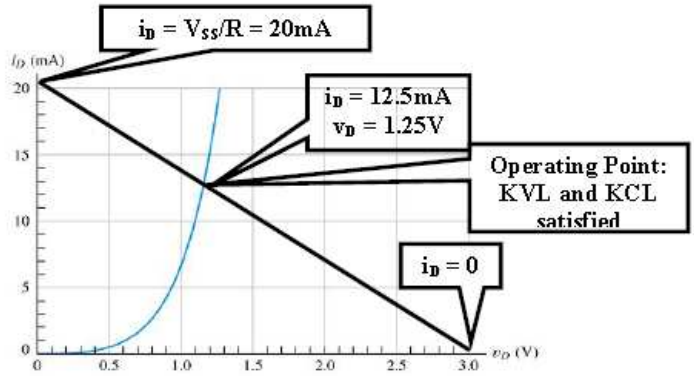
Assume : $V_{SS} = 3V$
and $R = 150\Omega$

When $v_D = 0$:

$$i_R = i_D = \frac{V_{SS}}{R} = 20mA$$

When $v_D = V_{SS}$:

$$i_R = i_D = 0$$



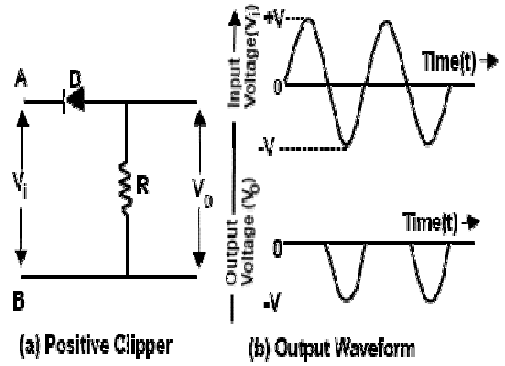
1.3 Clipping (limiting) circuit:

Clipping circuits are used to transmit a part of arbitrary waveform which lies above or below the reference level. Clipping circuits are also referred to as voltage (or current) limiters, amplitude selectors and voltage slicers. The clipper circuits are of the following types.

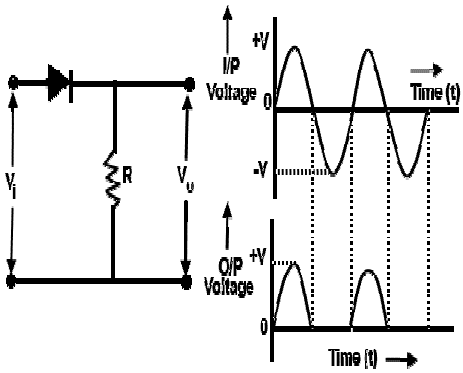
- Series positive clipper
- Series negative clipper
- Shunt or parallel clipper
- Shunt or parallel positive negative
- Clipper Dual (combination)Diode clipper

The series configuration is defined as one where the diode is in series with the load, while the parallel variety has the diode in a branch parallel to the load. The type of clipper combines a parallel negative clipper with negative bias (D_1 and B_2) and a parallel positive bias (D_1 and B_1). Hence the combination of a biased positive clipper and a biased negative clipper is called combination or dual diode clipper.

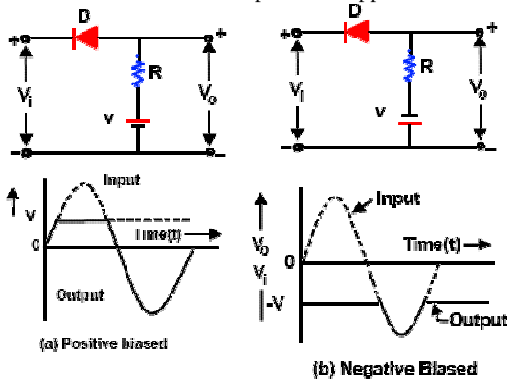
Example of series clipper:



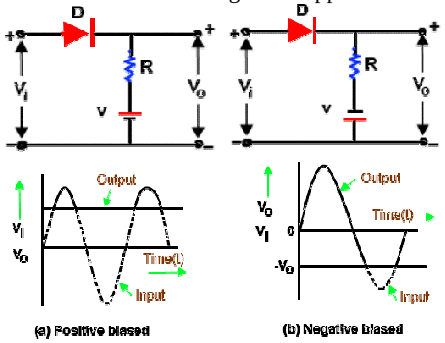
Series positive clipper



Series negative clipper

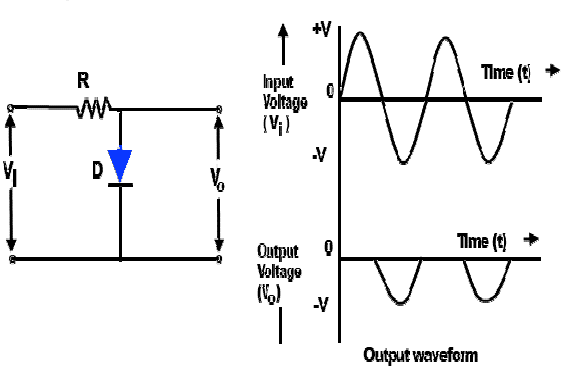


Series-positive clipper with bias

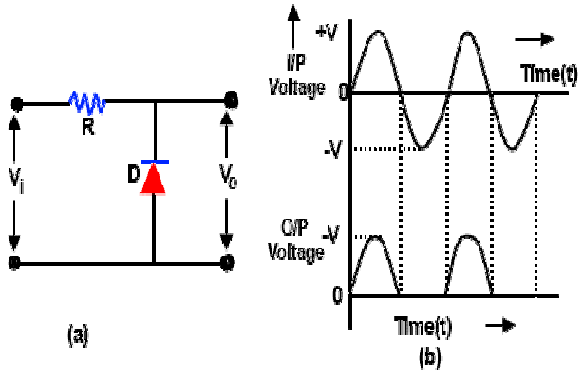


Series-negative clipper with bias

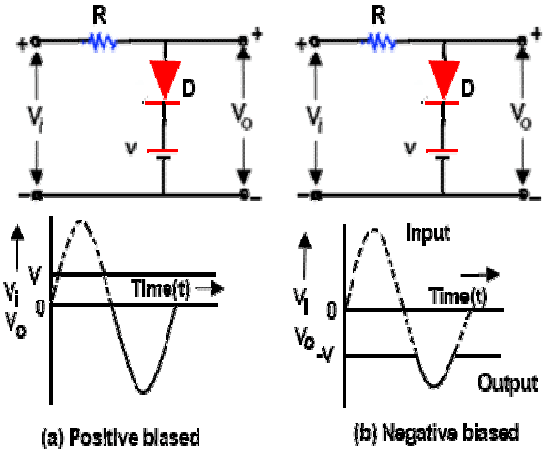
Example of parallel clipper:



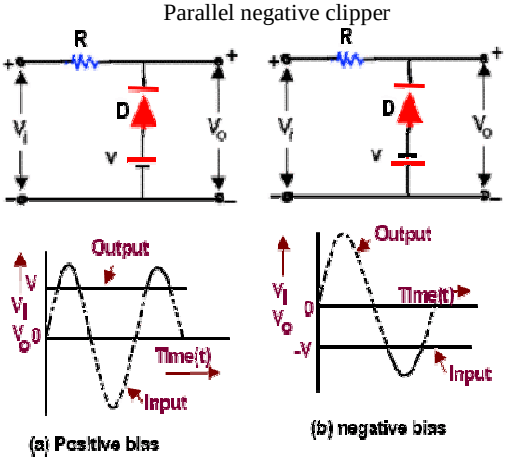
Parallel positive clipper



Parallel negative clipper

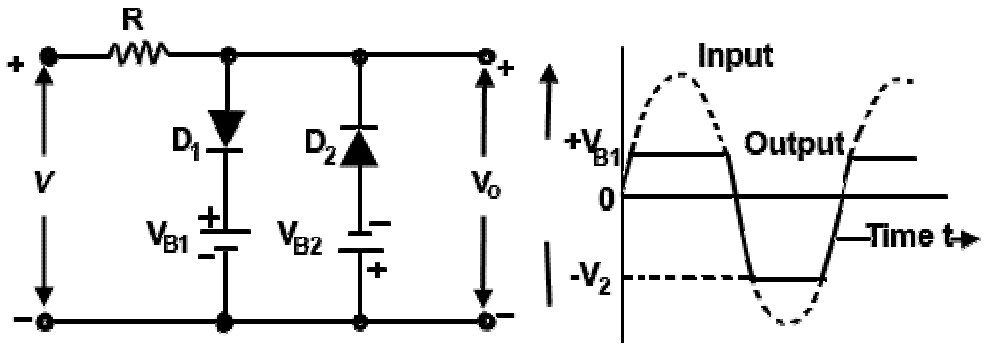


Parallel-positive clipper with bias(in negative bias condition v should be in reverse bias condition)



Parallel-negative clipper with bias

Example of parallel clipper:



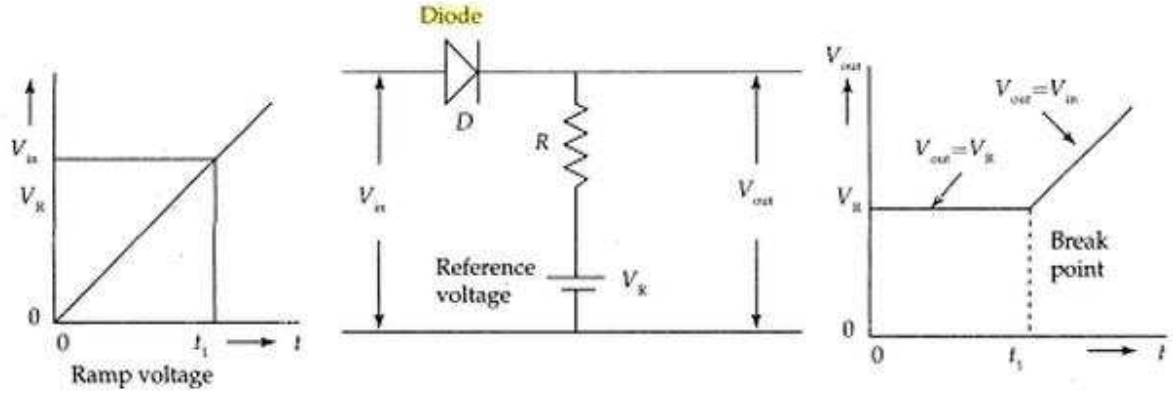
DUAL (COMBINATION) DIODE CLIPPER

1.4 Comparator:

A comparator is a device which is used to sense when an arbitrary varying signal reaches some threshold or reference level. Comparators find application in many electronics systems: for example, they may be used to sense when a linear ramp reaches some defined voltage level, or to indicate whether or not a pulse has amplitude greater than a particular value.

The non-linear circuits to perform the operation of clipping may also be used to perform the operation of comparison. The basic difference between the two is that in comparator there is no interest in reproducing any part of the signal waveform and desired portion of the input signal is reproduced in the output port of a clipping circuit without any change in desired wave shape.

The input signal to a comparator circuit is a ramp voltage linearly increases with time. The input waveform $v(t) = \alpha t$ for ramp type waveform

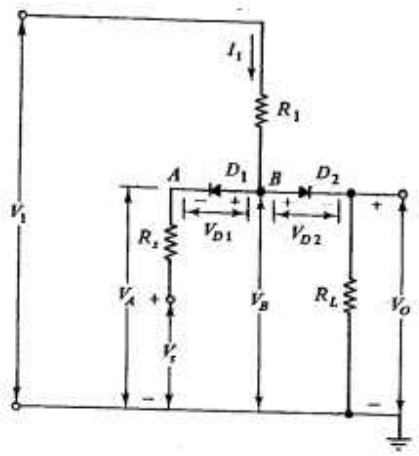


Circuit working:

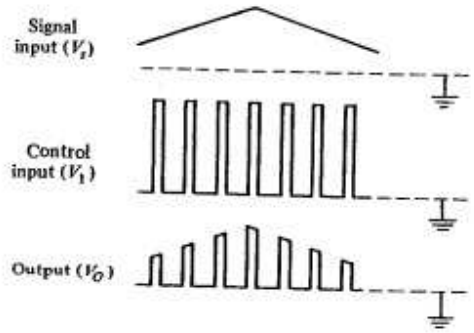
- At time $t < t_1$,the diode circuit is reverse biased as long as$V_{in} < V_R$. Hence the output voltage is equal to V_R from 0 instant to break pointt_1.
- From the time t=t_1, the diode is forward biased and act as a closed switched and the output follow the input i.e.$V_{out} = V_{in}$.
- Hence the output signal having amplitude greater than reference signal will appear at the output terminal and all other signal are blocked by the reversed biased diode circuit till the reference voltage is sensed.
- Due to the above feature, the diode is used as a comparator circuit to mark the instant at which V_{in} reachesV_R.

Sampling gate:

Sampling gate is a switching circuit which is employed to sample the amplitude of dc signal or low frequency signal. Sampling gate is constructed by using diodes, BJTs and FETs. A very simple diode circuit which is sampling a voltage signal is given in below figure.



(a) Circuit of diode sampling gate



(b) Voltage waveforms

Where V_S=source signal which is going to be sampled.

V_{in}=pulse control input is applied throughR_1.

V_o=output signal

R_s and $R_L$are the source and load resistance respectively.

When control voltage is zero or negative, the diodes D_1 and D_2 are reversed biased so $V_O \simeq 0$.when control voltage is zero, the diode voltage is positive, both the diodes are forward biased. So

$$V_A = V_S + I_S R_S$$

If$I_S R_s << V_S,\ V_A \simeq V_S$.

And $V_B = V_A + V_{D_1} \simeq V_S + V_{D_1}$

$$V_o = V_B - V_{D_2} \simeq V_S + V_{D_1} - V_{D_2}$$

$$\simeq V_S \quad \text{where} V_{D_1} = V_{D_2}.$$

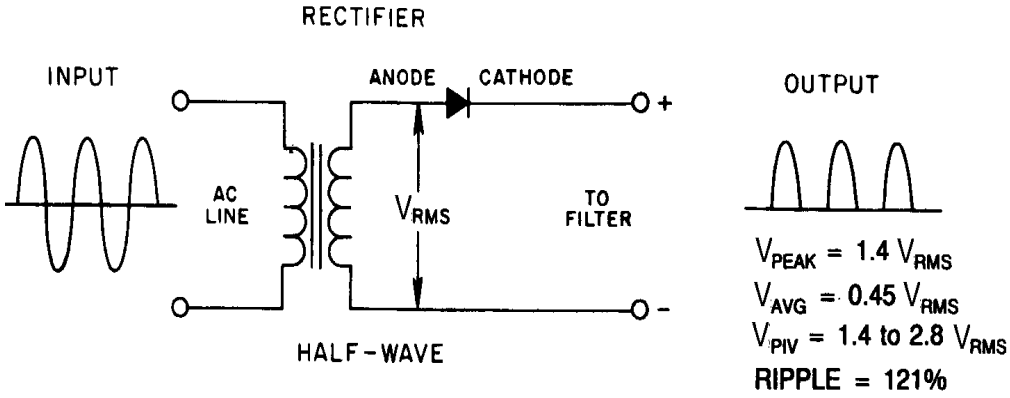
From the above analysis, we observed that the source signal is passed to the output signal when the control signal is positive. The diode sampling gate has error due to differences in voltage drops across the each diode and due to the leakage current in diode. It is applicable only where large signal amplitude is involved and where accuracy is not important.

Rectifiers:

A rectifier is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which flows in only one direction. The process is known as rectification.

I. Half Wave Rectifier:

The power diode in a half wave rectifier circuit passes just one half of each complete sine wave of the AC supply in order to convert it into a DC supply. Then this type of circuit is called a "half-wave" rectifier because it passes only half of the incoming AC power supply as shown below.



II. **Full Wave Rectifier**:

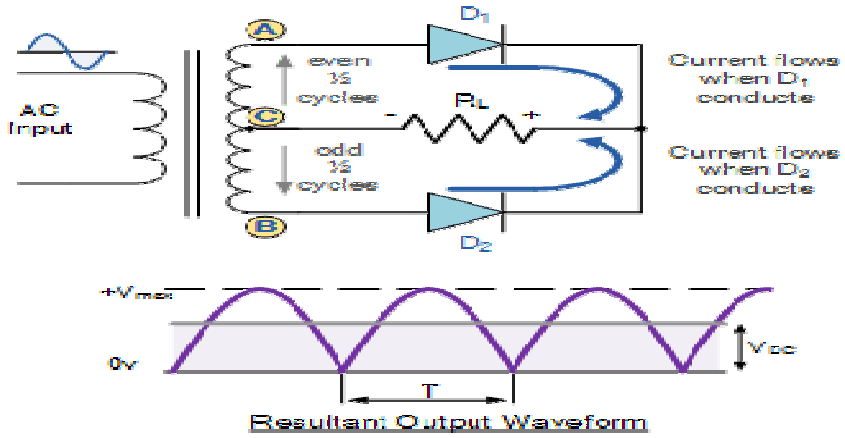
In a Full Wave Rectifier circuit two diodes are now used, one for each half of the cycle. A multiple winding transformer is used whose secondary winding is split equally into two halves with a common centre tapped connection, (C). This configuration results in each diode conducting in turn when its anode terminal is positive with respect to the transformer centre point C producing an output during both half-cycles, twice that for the half wave rectifier so it is 100% efficient as shown below.

a) Centre trap diode rectifier:

- The full wave rectifier circuit consists of two *power diodes* connected to a single load resistance (R_L) with each diode taking it in turn to supply

current to the load. When point A of the transformer is positive with respect to point C, diode D_1 conducts in the forward direction as indicated by the arrows.

- When point B is positive (in the negative half of the cycle) with respect to point C, diode D_2 conducts in the forward direction and the current flowing through resistor R is in the same direction for both half-cycles. As the output voltage across the resistor R is the phasor sum of the two waveforms combined, this type of full wave rectifier circuit is also known as a "bi-phase" circuit.
- The peak voltage of the output waveform is the same as before for the half-wave rectifier provided each half of the transformer windings have the same rms voltage value.
- The main disadvantage of this type of full wave rectifier circuit is that a larger transformer for a given power output is required with two separate but identical secondary windings making this type of full wave rectifying circuit costly compared to the "Full Wave Bridge Rectifier" circuit equivalent.

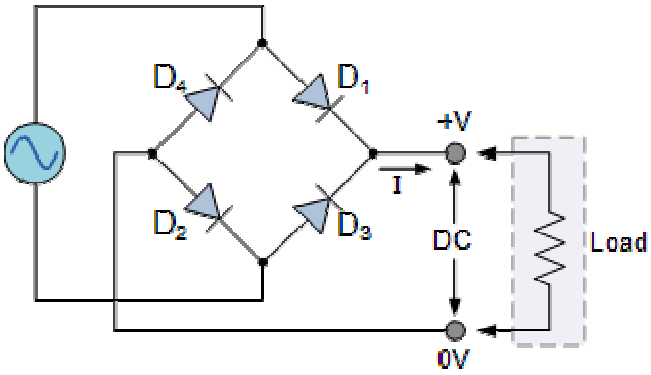


b) **Diode bridge rectifier:**

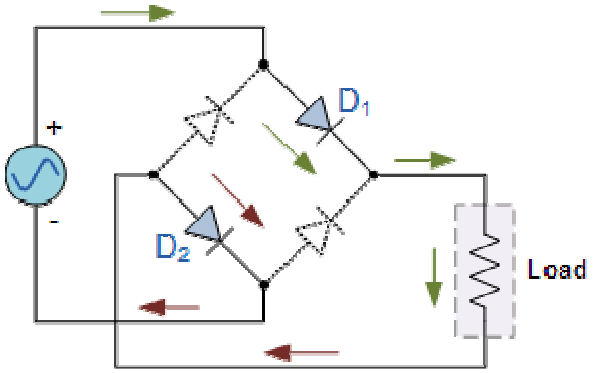
- Another type of circuit that produces the same output waveform as the full wave rectifier circuit above, is that of the Full Wave Bridge Rectifier. This type of single phase rectifier uses four individual rectifying diodes connected in a closed loop "bridge" configuration to produce the desired output. The main advantage of this bridge circuit is that it does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side.
- The four diodes labeled D_1 to D_4 are arranged in "series pairs" with only two diodes conducting current during each half cycle. During the positive half cycle of the supply, diodes D1 and D2 conduct in series while

diodes D3 and D4 are reverse biased and the current flows through the load as shown below.

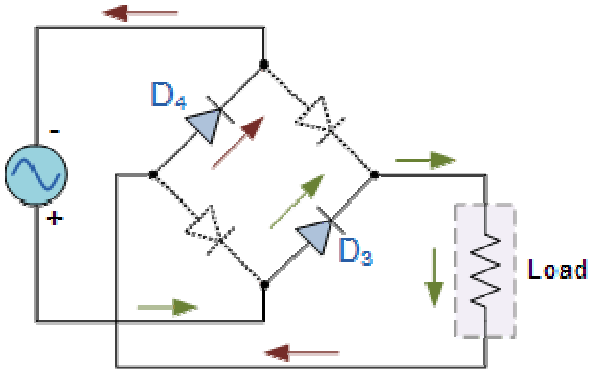
- During the negative half cycle of the supply, diodes D3 and D4 conduct in series, but diodes D1 and D2switch “OFF” as they are now reverse biased. The current flowing through the load is the same direction as before.



The Diode Bridge Rectifier



Bridge diode during positive half cycle



Bridge diode during negative half cycle

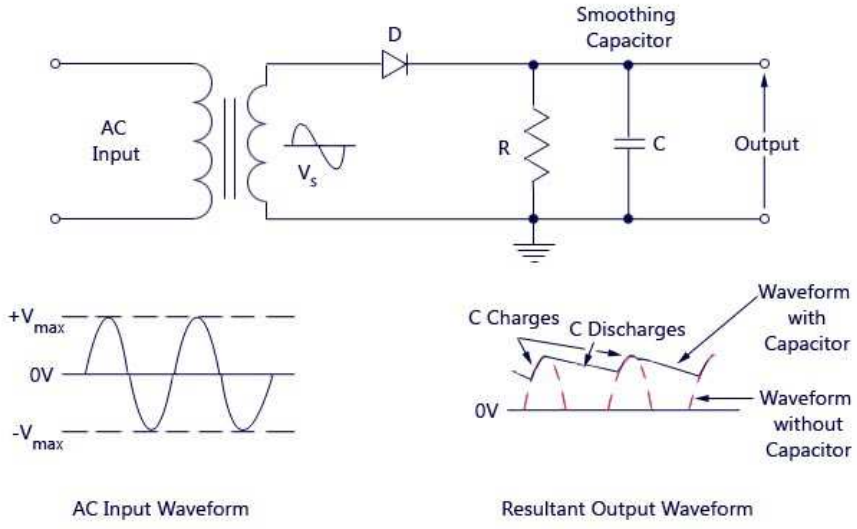
- The main disadvantage of a bridge rectifier is that it needs four diodes, two of which conduct in alternate half-cycles. Because of this the total voltage drop in diodes becomes double of that in case of centre-tap rectifier, losses are increased and rectification efficiency is somewhat reduced.

Capacitor filter:

Output of half wave rectifier is not a constant DC voltage (pulsating dc voltage with ac ripples) .In real life application; we need a power supply with smooth wave for (DC power supply with constant output voltage). A constant output voltage from the DC power supply is very important as it directly impacts the reliability of the electronic device we connect to the power supply. We

can make the output of half wave rectifier smooth by using a filter (a capacitor filter or an inductor filter) across the diode. In some cases a resistor-capacitor coupled filter (RC) is also used.

In this filter a capacitor is connected across the load during the rise of voltage cycle it gets charge and this charge is supply to the load during the fall in the voltage cycle. This process is repeated for each cycle and thus the repel is reduced across the load. It is popular, because of its low cost, small size, less weight and good characteristics.



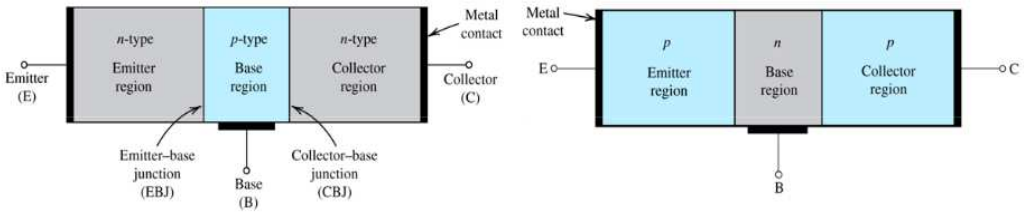
Half Wave Rectifier with Capacitor Filter – Circuit Diagram & Output Waveform

CHAPTER-2

(Lecture-3 to 6)

Junction transistor:

- Both electrons and holes participate in the conduction process for bipolar devices.
- BJT consists of two *pn* junctions constructed in a special way and connected in series, back to back.
- The transistor is a three-terminal device with emitter, base and collector terminals.
- From the physical structure, BJTs can be divided into two groups: ***npn*** and ***pnp*** transistors.



Modes of operation:

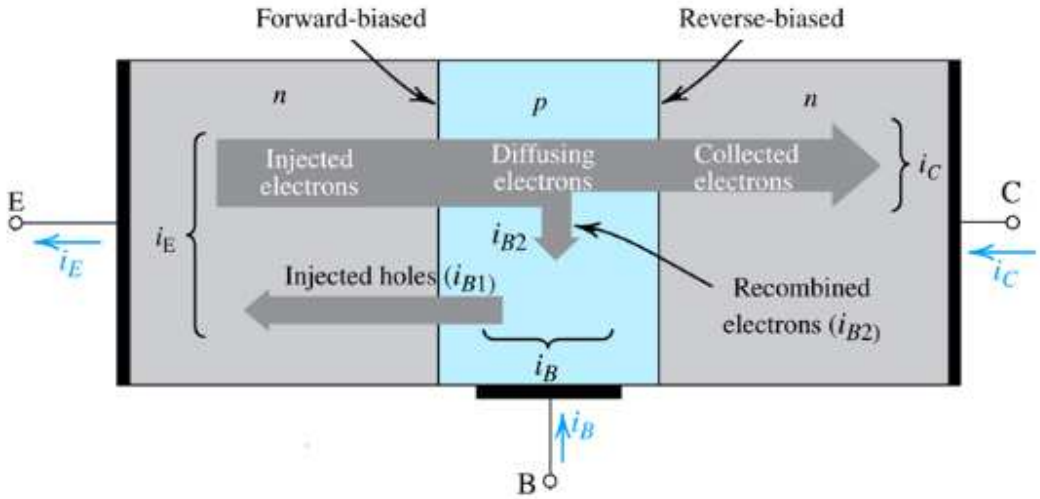
- The two junctions of BJT can be either forward or reverse-biased.
- The BJT can operate in different modes depending on the junction bias.
- The BJT can operate in different modes depending on the junction bias.
- Switching applications utilize both the cutoff and saturation modes.

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

Operation of the *npn* transistor in the active mode:

- Electrons in emitter regions are injected into base due to the forward bias at EBJ.
- Most of the injected electrons reach the edge of CBJ before being recombined if the base is narrow.
- Electrons at the edge of CBJ will be swept into collector due to the reverse bias at CBJ.
- Emitter injection efficiency$(\gamma) = {i_{En}}/{(i_{En} + i_{Ep})}$

- Base transport factor$(\alpha_T) = {}^{i_{Cn}}/_{i_{En}}$
- Base transport factor$(\alpha) = {}^{i_{Cn}}/_{i_E} = \gamma\alpha_T < 1$
- Terminal currents of BJT in active mode:
  i_E(Emitter current) = i_{En}(electron injection from E to B) + i_{Ep}(hole injection from B to E)
  i_C(Collector current) = i_{Cn}(electron drift) + i_{CBO}(CBJ reverse saturation current with emitter open)
  i_B(Base current) = i_{B1}(hole injection from B to E) + i_{B2}(recombination in base region)



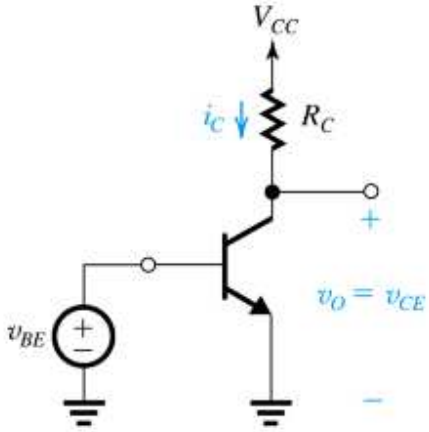
The transistor as an amplifier:

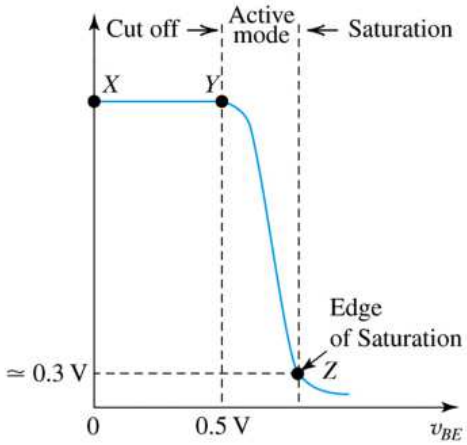
- A BJT circuit with a collector resistor R_C can be used as a simple voltage amplifier.
- Base terminal is used the amplifier input and the collector is considered the amplifier output.
- The voltage transfer characteristic (VTC) is obtained by solving the circuit from low to highV_{BE}.
- Cutoff mode:
  $0V \leq V_{BE} < 0.5V$ & $i_C = 0$
  $V_O = V_{CE} = V_{CC}$
- Active mode:
  $V_{BE} > 0.5V$ & $i_C \neq 0$
  $V_O = V_{CC} - i_C R_C$

- Saturation mode:
  V_{BE} further increases

$V_{CE} = V_{CE(sat)} = 0.2V$

$V_O = 0.2V$





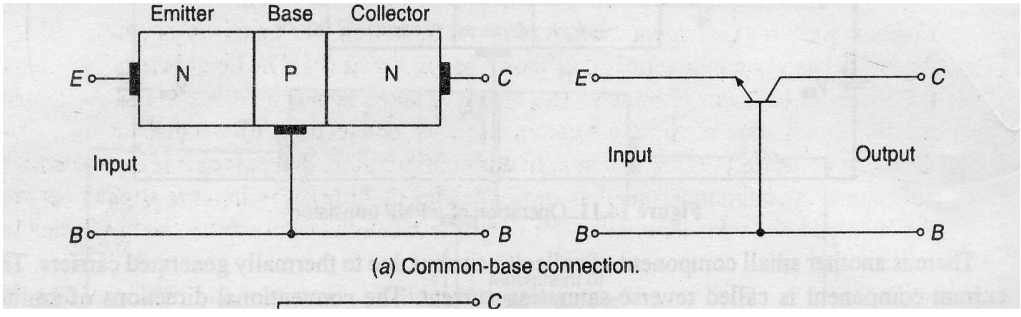
Transistor Configuration:

Depending upon the terminals which are used as a common terminal to the input and output terminals, the transistors can be connected in the following three different configuration.

1. common base configuration
2. common emitter configuration
3. common collector configuration

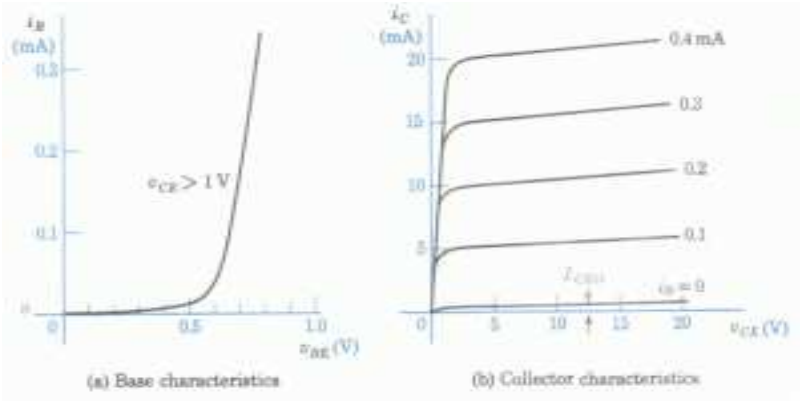
Common base configuration:

- In this configuration base terminal is connected as a common terminal.
- The input is applied between the emitter and base terminals. The output is taken between the collector and base terminals.



- Input characteristics: The output (CB) voltage is maintained constant and the input voltage (EB) is set at several convenient levels. For each level of input voltage, the input current $\mathbf{I_E}$ is recorded. $\mathbf{I_E}$ is then plotted versus $\mathbf{V_{EB}}$ to give the common-base input characteristics.

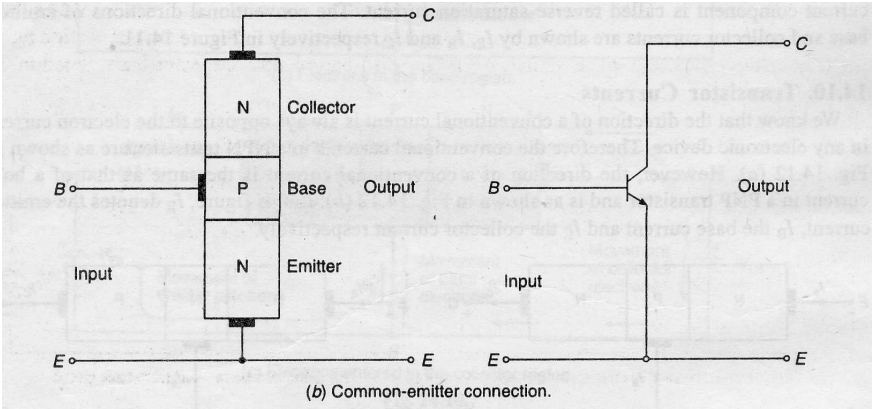
- Output characteristics: The emitter current $\mathbf{I_E}$ is held constant at each of several fixed levels. For each fixed value of $\mathbf{I_E}$, the output voltage $\mathbf{V_{CB}}$ is adjusted in convenient steps and the corresponding levels of collector current $\mathbf{I_C}$ are recorded. For each fixed value of $\mathbf{I_E}$, $\mathbf{I_C}$ is almost equal to $\mathbf{I_E}$ and appears to remain constant when $\mathbf{V_{CB}}$ is increased.



(a) Base characteristics (b) Collector characteristics

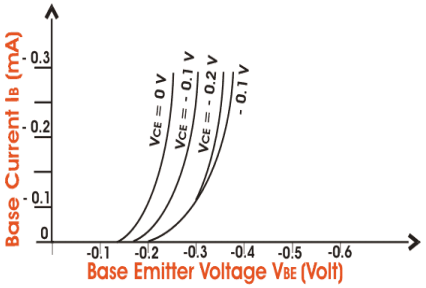
Common emitter configuration:

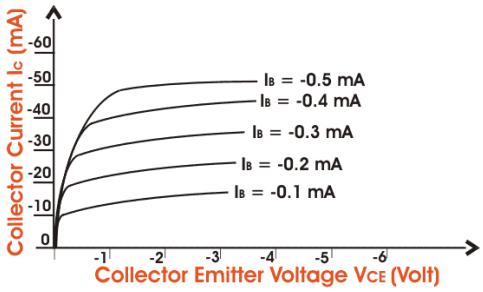
- In this configuration emitter terminal is connected as a common terminal.
- The input is applied between the emitter and base terminals. The output is taken between the collector and base terminals.



(*b*) Common-emitter connection.

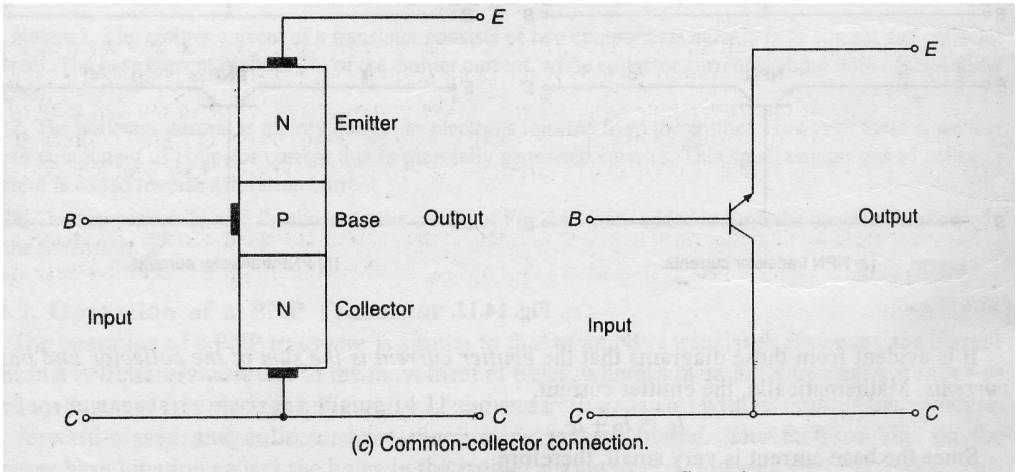
- Input characteristics: The output voltage $\mathbf{V_{CE}}$ is maintained constant and the input voltage $\mathbf{V_{BE}}$ is set at several convenient levels. For each level of input voltage, the input current $\mathbf{I_B}$ is recorded. $\mathbf{I_B}$ is then plotted versus $\mathbf{V_{BE}}$ to give the common-base input characteristics.
- Output characteristics: The Base current $\mathbf{I_B}$ is held constant at each of several fixed levels. For each fixed value of $\mathbf{I_B}$, the output voltage $\mathbf{V_{CE}}$ is adjusted in convenient steps and the corresponding levels of collector current $\mathbf{I_C}$ are recorded. For each fixed value of $\mathbf{I_B}$, $\mathbf{I_C}$ level is Recorded at each $\mathbf{V_{CE}}$ step. For each $\mathbf{I_B}$ level, $\mathbf{I_C}$ is plotted versus $\mathbf{V_{CE}}$ to give a family of characteristics.





Common collector configuration:

- In this configuration collector terminal is connected as a common terminal.
- The input is applied between the base and collector terminals. The output is taken between the emitter and collector terminals.

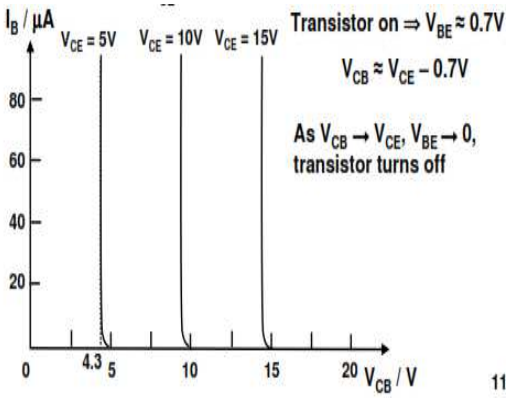


- Input characteristics: The common-collector input characteristics are quite different from either common base or common-emitter input characteristics. The difference is due to the fact that the input voltage **(V_{BC})** is largely determined by **(V_{EC})** level.

$$V_{EC} = V_{EB} + V_{BC}$$

$$V_{EB} = V_{EC} - V_{BC}$$

- Output characteristics: The operation is much similar to that of C-E configuration. When the base current is I_{CO}, the emitter current will be zero and consequently no current will flow in the load. When the base current is increased, the transistor passes through active region and eventually reaches saturation. Under the saturation conditions all the supply voltage, except for a very small drop across the transistor will appear across the load resistor.



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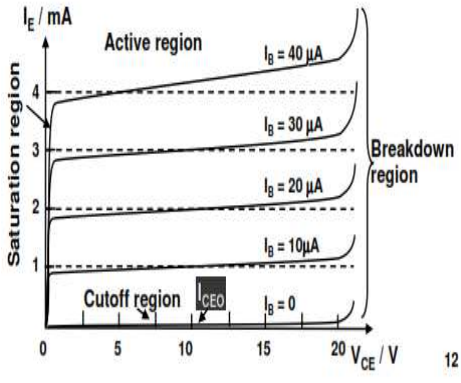
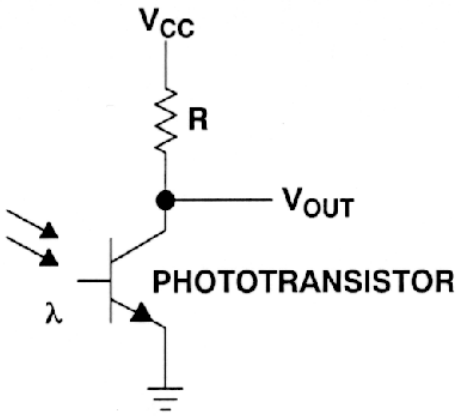


12

Phototransistor:

The phototransistor is much sensitive semiconductor photo device than the p-n photodiode. it is usually connected in common-emitter configuration with the base open and radiation is concentrated on the region near the collector junction.



CHAPTER-3
(Lecture-7 to 10)

Transistor at low frequencies:

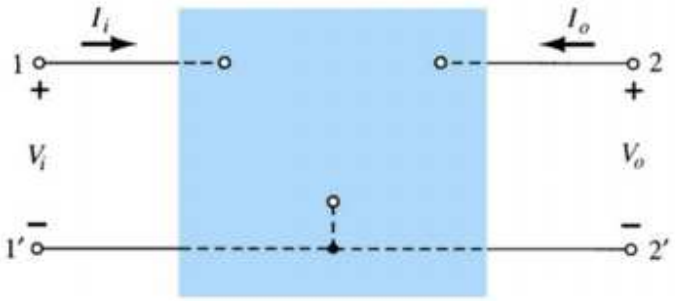
The transistor can be employed as an amplifying device, that is, the output ac power is greater than the input ac power. The factor that permits an ac power output greater than the input ac power is the applied DC power. The amplifier is initially biased for the required DC voltages and currents. Then the ac to be amplified is given as input to the amplifier. If the applied ac exceeds the limit set by dc level, clipping of the peak region will result in the output. Thus, proper (faithful) amplification design requires that the dc and ac components be sensitive to each other's requirements and limitations. The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system.

BJT Transistor modeling:

- A model is an equivalent circuit that represents the AC characteristics of the transistor.
- A model uses circuit elements that approximate the behavior of the transistor.
- There are two models commonly used in small signal AC analysis of a transistor:
  i. r_e model
  ii. Hybrid equivalent model

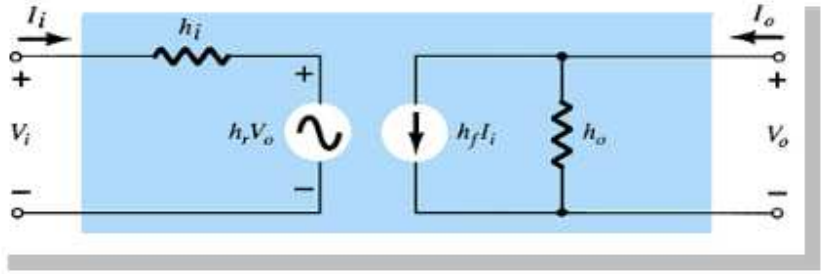
Two port device and hybrid model:

- For the hybrid equivalent model, the parameters are defined at an operating point.
- The quantitiesh_{ie},h_{re},h_{fe}, and h_{oe} are called hybrid parameters and are the components of a small – signal equivalent circuit.
- The description of the hybrid equivalent model will begin with the general two port system.

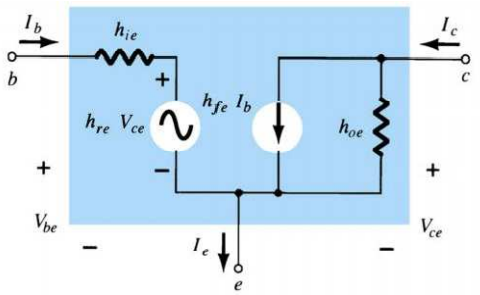


- $V_i = h_{11}I_i + h_{12}V_o$ & $I_o = h_{21}I_i + h_{22}V_o$

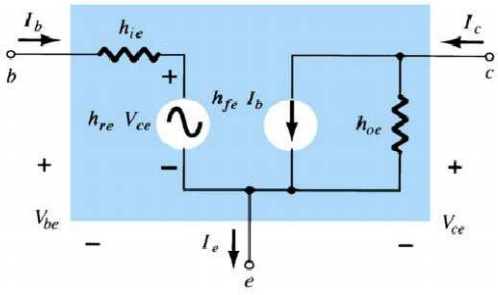
- The four variables h_{11}, h_{12}, h_{21} and h_{22} are called hybrid parameters (the mixture of variables in each equation results in a "hybrid" set of units of measurement for the h – parameters).
- $h_{11} = h_i$ (input resistance)$= {V_i}/{I_i}\Big|_{V_o=0}$
- $h_{12} = h_r$(reversed voltage gain)$= {V_i}/{V_o}\Big|_{I_i=0}$
- $h_{21} = h_f$(forward current gain)$= {I_o}/{I_i}\Big|_{V_o=0}$
- $h_{22} = h_o$(output admittance)$= {I_o}/{V_o}\Big|_{I_i=0}$



Hybrid equivalent circuit



Common Base configuration - hybrid equivalent circuit



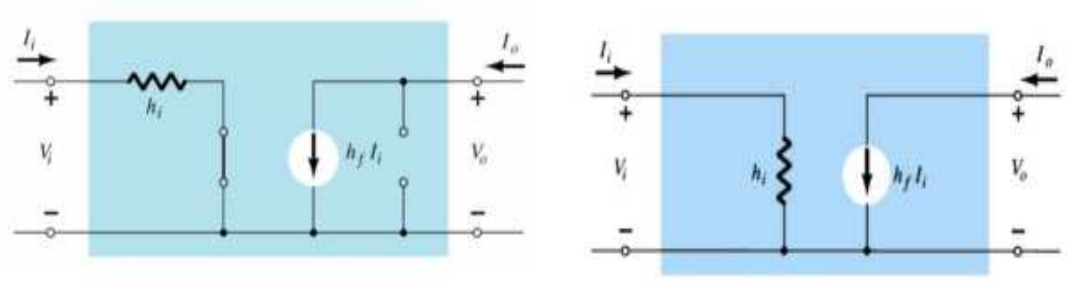
Common Emitter configuration - hybrid equivalent circuit

- Essentially, the transistor model is a three terminal two – port system.
- The h – parameters, however, will change with each configuration.
- To distinguish which parameter has been used or which is available, a second subscript has been added to the h – parameter notation.
- For the common – base configuration, the lowercase letter b is added, and for common emitter and common collector configurations, the letters e and c are used respectively.

Configuration	I_i	I_o	V_i	V_o
Common emitter	I_b	I_c	V_{be}	V_{ce}
Common base	I_e	I_c	V_{eb}	V_{cb}
Common Collector	I_b	I_e	V_{be}	V_{ec}

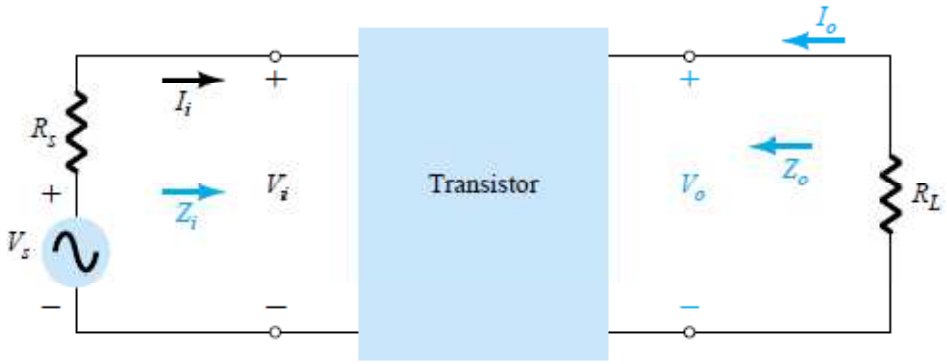
Input and output current and voltage of different transistor configuration in terms of h-parameter

- Normally h_r is a relatively small quantity, its removal is approximated by h_r and $h_r V_o$ = 0, resulting in a short – circuit equivalent.
- The resistance determined by $1/h_0$ is often large enough to be ignored in comparison to a parallel load, permitting its replacement by an open – circuit equivalent.

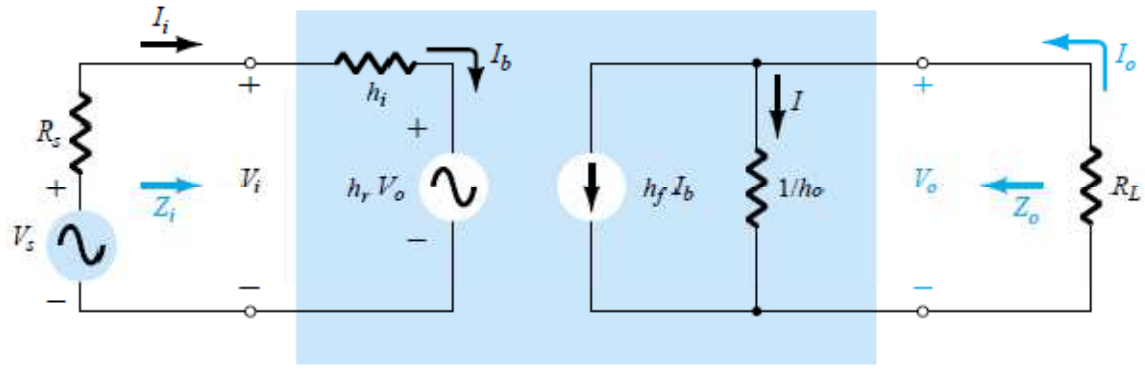


Simplified structure of hybrid model

Analysis of transistor amplifier using h-parameter:



Two-port system



Substituting the complete hybrid equivalent circuit into the two-port system

For analysis of transistor amplifier we have to determine the following terms:

- Current Gain(A_i)=I_o/I_i
- Voltage gain(A_V)=V_o/V_i
- Input impedance(Z_i)=V_i/I_i
- Output impedance(Z_o)=V_o/I_o

Current Gain:

Applying Kirchhoff's current law to the output circuit of the hybrid equivalent circuit

$I_0 = I + h_f I_b = V_0 / (1/h_o) + h_f$

$I_o = V_o h_o + h_f I_b$

Substituting $V_o = -I_o R_L$ gives us

$I_o = h_f I_b - h_o I_o R_L$

Rewriting the above equation we have

$I_o(1 + h_o R_L) = h_f I_b$

So that $A_i = I_o/I_b = h_f/(1 + h_o R_L)$

Note that the current gain will reduce to the familiar result of $A_i = h_f$ if the factor $h_o R_L$ is sufficiently small compared to 1.

Voltage gain:

Applying Kirchhoff's voltage law to the input circuit results in

$V_i = h_i I_b + h_r V_o$

Substituting $I_b = {(1 + h_o R_L)}/{h_f}$ and $I_o = -{V_o}/{R_L}$ in the above equation and solving for ${V_o}/{V_i}$

we get $A_v = {-h_f R_L}/{h_i + (h_i h_o - h_f h_r) R_L}$

In this case, the familiar form $A_v = {-h_f R_L}/{h_i}$ of will return if the factor $(h_i h_o - h_f h_r) R_L$ is sufficiently small compared to *hi*.

Input impedance:

For the input circuit, $V_i = h_i I_b + h_r V_o$

Substituting $I_o = -{V_o}/{R_L}$, $A_i = {I_o}/{I_b}$

So that the equation above becomes $V_i = h_i I_b - h_r R_L A_i I_b$

Solving for the ratio ${V_i}/{I_b}$, we obtain

$Z_i = {V_i}/{I_b} = h_i - h_r R_L A_i$ (substitute A_i in the equation)

Output impedance:

The output impedance of an amplifier is defined to be the ratio of the output voltage to the output current with the signal V_s set to zero. For the input circuit with V_s=0,

$I_i = {-h_r V_o}/{R_s + h_i}$

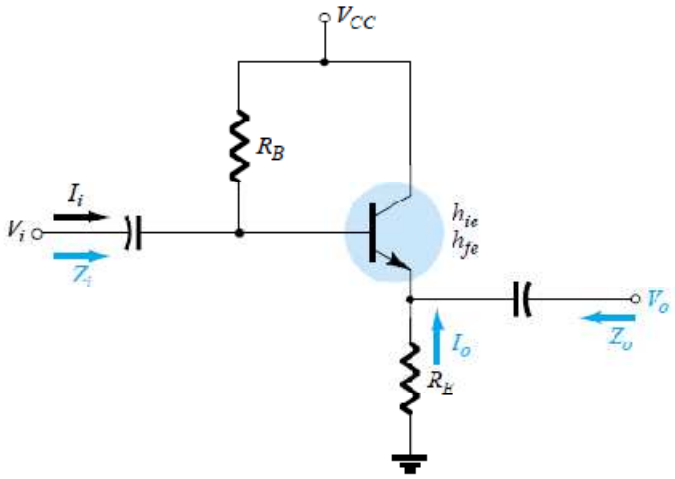
Substituting this relationship into the following equation obtained from the output circuit yields

$I_o = V_o h_o + h_f I_b$

And $Z_o = {V_o}/{I_o} = {1}/{h_o - ({h_f h_r}/{(h_i + R_S)})}$

In this case, the output impedance will reduce to the familiar form $Z_o = {1}/{h_o}$ for the transistor when the second factor in the denominator is sufficiently smaller than the first.

Emitter-Follower:



Emitter-follower configuration

- The above configuration is called as emitter follower because its voltage gain is nearly equal to unity i.e.$V_o \simeq V_i$ which means change in input voltage is nearly equal to change in output voltage.
- In this configuration emitter follows the input signal. Here input resistance is very high i.e. in the range of kilos and output voltage is very low i.e. in the range of tens of ohms.
- Hence common use of common collector is as a buffer stage which transfers resistance from high to low resistance over a wide range of frequency with voltage gain of unity.
- It also increases the power level of signal.

$$A_I = {}^{-I_e}/_{I_b} = {}^{-h_{fc}}/_{1 + h_{oc}R_L}$$

$$Z_i = {}^{V_i}/_{I_b} = h_{ie} + h_{re}A_iR_L$$

$$A_V = {}^{V_o}/_{V_i} = A_I \, {}^{R_L}/_{R_i}$$

$$Y_o = h_{oc} - {}^{h_{fc}h_{rc}}/_{h_{ic} + R_s}$$ Where R_s and R_L is source and load resistance.

Miller's theorem and its dual:

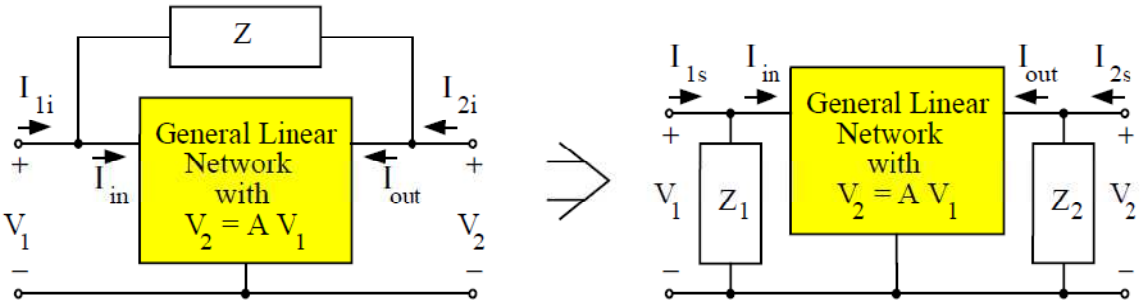
- The introduction of an impedance that connects amplifier input and output ports adds a great deal of complexity in the analysis process. One technique that often helps reduce the complexity in some circuits is the use of ***Miller's theorem***.
- Miller's theorem applies to the process of creating equivalent circuits. This general circuit theorem is particularly useful in the high-frequency analysis of certain transistor amplifiers at high frequencies.
- Miller's Theorem generally states:

Given any general linear network having a common terminal and two terminals whose voltage ratio, with respect to the common terminal, is given by:

$$V_2 = AV_1$$

- If the two terminals of the network are then interconnected by impedance, Z, an equivalent circuit can be formed. This equivalent circuit consists of the same general linear network and two impedances; each of which shunts a network terminal to common terminal. These two impedances have value

$Z_1 = {Z}/{1 - A}$ And $Z_2 = {AZ}/{1 - A}$



(a) (b)

Miller Equivalent Circuits

(a) Interconnecting Impedance (b) Port-Shunting Impedances

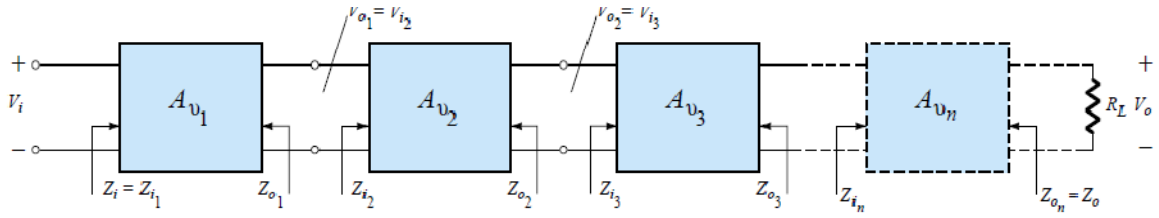
Cascading transistor amplifier:

The two-port system approach is particularly useful for cascaded systems where A_{v1}, A_{v2}, A_{v3} and so on, are the voltage gains of each stage under loaded conditions that is $A_{v1}$is determined with the input impedance to A_{v2}acting as the load onA_{v1}. ForA_{v2}, A_{v1} will determine the signal strength and source impedance at the input to A_{v2} . The total gain of the system is the determined by the product of the individual gains as follows:

$$A_{vT} = A_{v1}A_{v2}A_{v3}\cdots$$

and the total current gain by

$$A_{iT} = -A_{vT}\,{Z_{iL}}/{R_L}$$



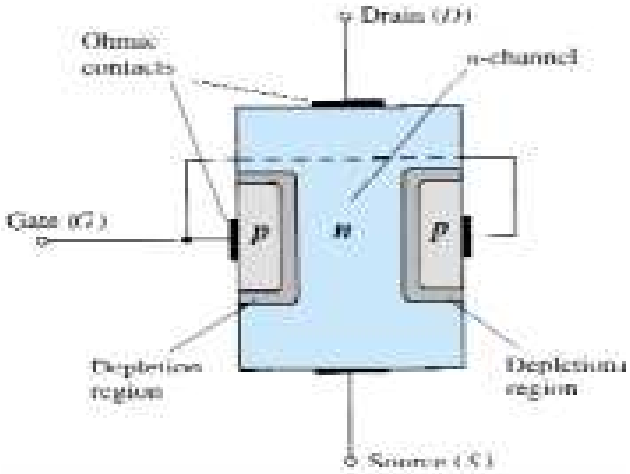
Cascade system

CHAPTER-4

(Lecture-11 to 14)

JFET (Junction FET):

The FET is a three terminal (i.e. drain, gate and source), unipolar voltage controlled device. There are two types of such devices MOSFET (Metal Oxide Semiconductor FET) and JFET (Junction FET). Again the JFET is classified into n-channel JFET where current conduction occurred due to electrons and p-channel JFET where current conduction occurred due to holes. In JFET gate to source junction is always in reversed bias condition and drain is always high potential than source.



Junction field-effect transistor (JFET)

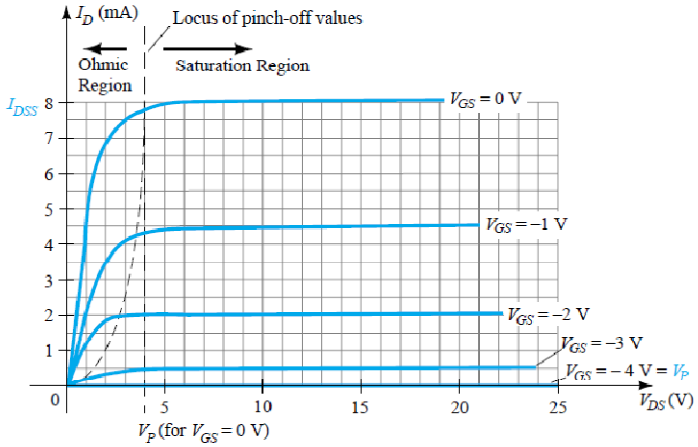
Advantages of JFET:

- Very high input impedance order of $10^8 - 10^{10}$ ohm.
- Operation of JFET depends on the bulk material current carriers that do not cross junctions.
- Very high power gain.
- Smaller in size and having high efficiency.

V-I characteristics of JFET:

As JFET is a voltage controlled device, its drain current is depend upon the gate to source voltage and drain to source voltage i.e.I_D(drain current) is a function of V_{GS}(gate to source voltage) and V_{DS}(drain to source voltage).

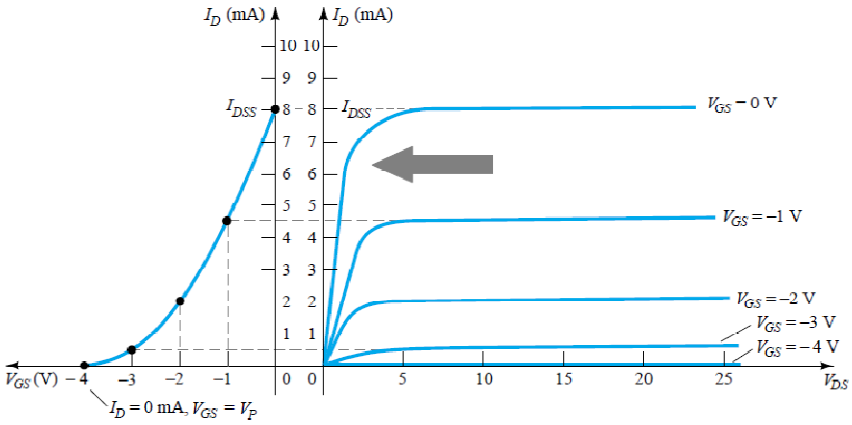
$$\text{Where} I_D = I_{Dss}(1 - {V_{GS}}/{V_{GS(cut\ off)}})^2, V_{GS(cutoff)} = V_P$$



Drain characteristic
n-Channel JFET characteristics with$I_{DSS} = 8mA$ and$V_P = -4$

- I_{DSS} is the maximum drain current for a JFET and is defined by the conditions V_{GS}=0 and $V_{Ds} > V_P$ where V_P is the pinch off voltage.
- For gate-to-source voltages V_{GS} less than (more negative than) the pinch-off level, the drain current is 0 A ($I_D = 0A$).
- For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively.

Transfer characteristics:
The transfer characteristics of JFET is between I_D versus V_{GS} when V_{Ds} is kept constant.



Transfer Characteristics

- When V_{GS} =0 V, I_D =I_{DSS}.
- When $V_{GS} = V_P$, I_D = 0 mA.

FET small signal model:

The ac analysis of an FET configuration requires that a small-signal ac model for the FET. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source. The three major component of ac model are as follows:

- Drain resistance (r_D) - It is the ratio of change in drain – source voltage to the change in drain current at constant gate source voltage.

$$r_D = {\Delta V_{DS}}/{\Delta I_D}\Big|_{\Delta V_{GS}=constant}$$

- Transconductance(g_m) - it is the ratio of change in drain current to the change in gate source voltage at constant drain source voltage.

$$g_m = {\Delta I_D}/{\Delta V_{GS}}\Big|_{\Delta V_{DS}=constant}$$

$$\text{So } g_m = {-2I_{DSS}}/{V_{GS(cutoff)}}\left(1 - {V_{GS}}/{V_{GS(cutoff)}}\right)$$

- Amplification factor (μ) - it is the ratio of change in drain source voltage to the change in gate source voltage at constant drain current.

$$\mu = {\Delta V_{DS}}/{\Delta V_{GS}}$$

$$\text{So } \mu = r_D \times g_m$$

JFET biasing:

For the JFET to operate as a linear amplifier, the Q-point should be in the middle of the saturation region, the instantaneous operating point must at all times be confined to the saturation region, and the input signal must be kept sufficiently small. For selection of an appropriate operating point for a JFET amplifier stage proper biasing is needed. Similar to BJT, JFET is having three types of DC biasing.

- Fixed-bias configuration
- Self-bias configuration
- Voltage-divider configuration

FET as voltage variable resistor:

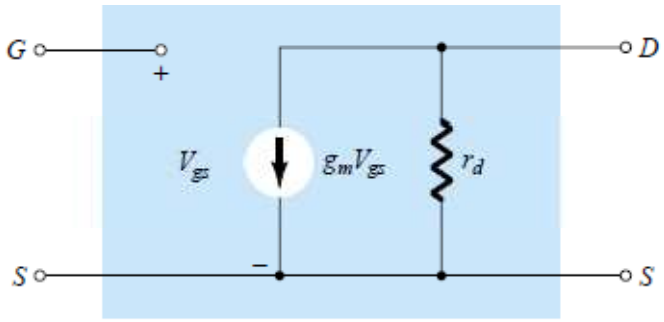
- FET is operated in the constant current portion of its output characteristics for the linear applications.

- In the region before pinch off, where V_{DS} is small the drain to source resistance r_d can be controlled by the bias voltageV_{GS}. In this region, FET is useful as a voltage variable resistor (VVR) or Voltage Dependent resistor.
- In JFET the drain source conductance $g_d$for small values of V_{DS} which may be expressed as $g_d = g_{do}[1 - ({}^{V_{GS}}/_{V_P})^{1}/_{2}]$where g_{do} is the value of drain conductance when the bias voltage $V_{GS}$is zero.
- The variation of the rd with V_{GS} can be closely approximated by $r_{d={}^{r_o}/_{(1-KV_{GS})}}$ r_o is drain resistance at zero gate bias and K constant dependent upon FET type.
- Small signal FET drain resistance rd varies with applied gate voltage $V_{GS}$and FET act like a variable passive resistor.

Common drain amplifier:

FET AC Equivalent Circuit:

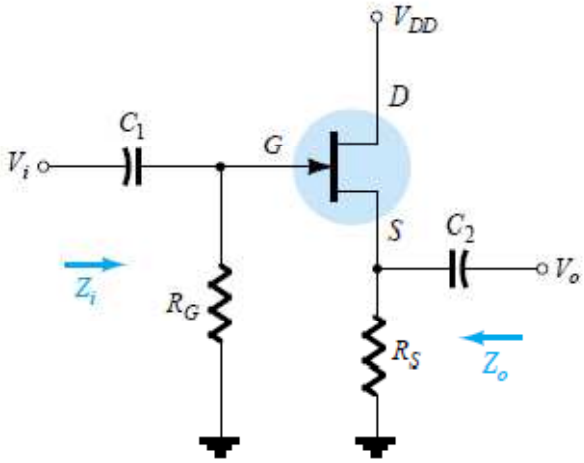
$$I_D = g_m V_{gs} + {}^{1}/_{r_d} V_{ds}$$



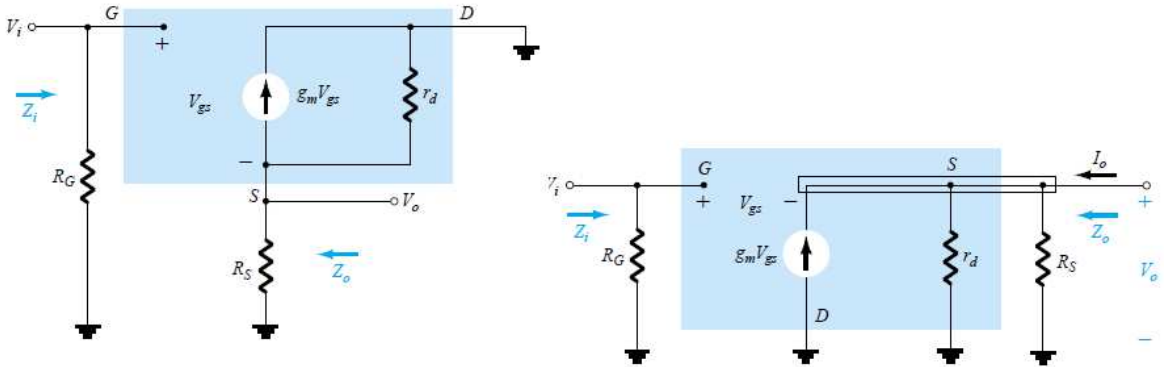
FET ac equivalent circuit

JFET source follower (common drain) configuration:

In a CD amplifier configuration the input is on the gate, but the output is from the source.

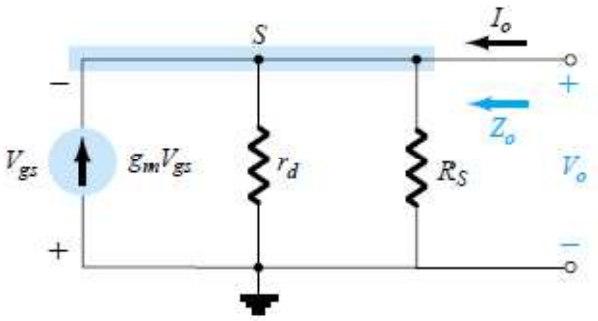


AC equivalent circuit of CD amplifier



CD ac equivalent circuit

- Input impedance: $Z_i = R_G$
- Output impedance: Setting V_i=0V will result in the gate terminal being connected directly to ground as shown in figure below.



Determining $Z_o$of the above diagram

$$Z_o = {V_o}/{I_o} = {V_o}\Big/{V_o\left(\frac{1}{r_d} + \frac{1}{R_s} + g_m\right)}$$

which has the same format as the total resistance of three parallel resistors. Therefore,

$$Z_o = r_d \| R_s \| \frac{1}{g_m}$$

For $r_d \geq 10R_s$, $Z_o = r_d \| R_s$

- Voltage gain:

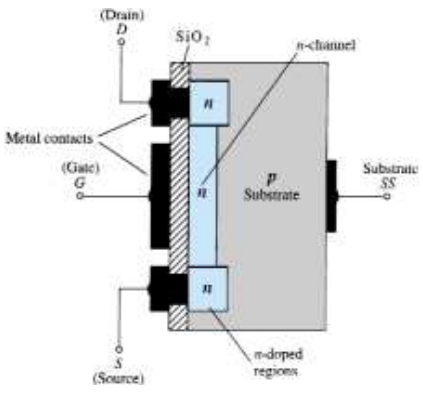
$$A_V = \frac{V_o}{V_i} = {g_m(r_d \| R_S)}\Big/{1 + g_m(r_d \| R_S)}$$

$$A_V = {g_m R_s}/{1 + g_m R_s}\Big|_{r_d \geq 10R_s}$$

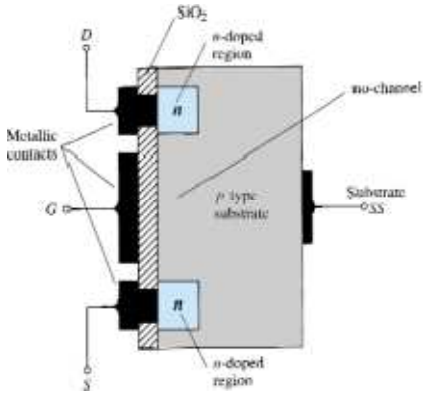
Since denominator is larger by a factor of one, the gain can never be equal to or greater than one.

MOSFET:

- MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a unipolar , voltage controlled current device and is a device in which current at two electrodes drain and source is controlled by the action of electric field at another electrode gate having in between a semiconductor very a thin metal oxide layer. MOSFET is classified into two types i.e. enhancement type and depletion type.
- There is no direct electrical connection between the gate terminal and the channel of a MOSFET. It is the insulating layer of SiO_2in the MOSFET construction that account for the very desirable high input impedance of the device.

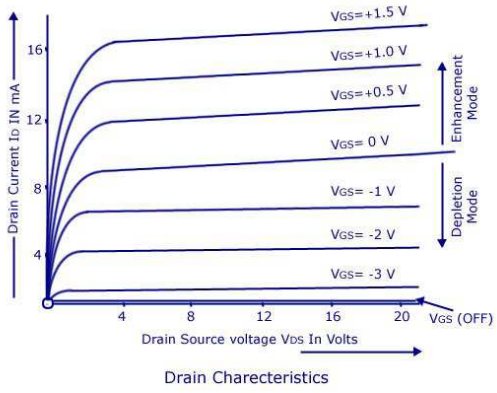


n-Channel depletion-type MOSFET.

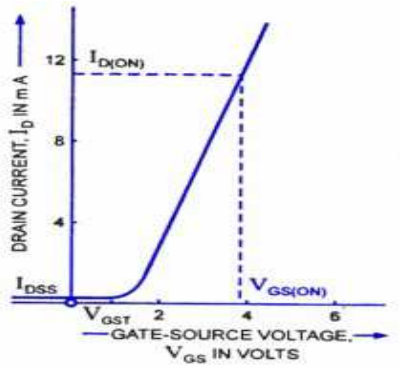


n-Channel enhancement-type MOSFET.

- Although there are some similarities in construction and mode of operation between depletion type and enhancement type but in case of depletion type there is a channel between source and drain terminals which is absent in case of enhancement type.
- The transfer function of depletion type MOSFET is same as the JFET transfer function.
- MOSFET can be operated with either a positive or a negative gate. When gate is positive with respect to the source it operates in the enhancement—or E-mode and when the gate is negative with respect to the source, it operates in depletion-mode.



Drain Charecteristics



Transfer Characteristic

- The equation for the transfer characteristic of E-MOSFETs is given as:

$$I_D = K(V_{GS} - V_{GS(Th)})^2$$

where I_D=Drain current

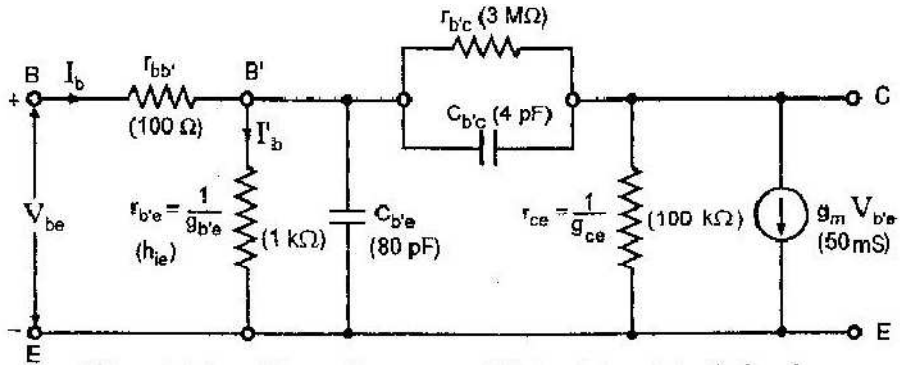
V_{GS}=Gate to source voltage

$V_{GS(Th)}$= Threshold voltage

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(Th)})^2}$$

The Hybrid-pi CE Transistor Model:

- The hybrid-pi or Giacoletto model of common emitter transistor model is given below. The resistance components in this circuit can be obtained from the low frequency h-parameters.
- For high frequency analysis transistor is replaced by high frequency hybrid-pi model and voltage gain, current gain and input impedance are determined.



The hybrid -pi model for a transistor in CE configuration

- $r_{b'b}$=ohmic base spreading resistance
- $v_{b'e}$=small change in voltage across base emitter junction
- $r_{b'e}$=resistance between B' and E
- $c_{b'e}$=diffusion capacitance between B' and E
- $r_{b'c}$= resistance between B' and C
- $c_{b'c}$= diffusion capacitance between B' and C
- r_{ce}= resistance between C and E
- $g_m v_{b'e}$=current generator

Hybrid -pi conductance and capacitance:

All the resistance components in the hybrid-pi model can be obtained from the h parameters in CE configuration.

- Transistor Transconductance(g_m)=$|I_C| / V_T$

  where I_C=collector current in mA

  V_T=thermal voltage which is nearly equally to 26mA at room temperature.

- The Input Conductance($g_{b'e}$)= $h_{fe} V_T / |I_C| = g_m / h_{fe}$

  where h_{fe}=short circuit current gain of CE configuration

- The Feedback Conductance($g_{b'c}$)= $h_{re} g_{b'e}$

  where h_{re}=reverse voltage gain when the input is open-circuited.

- The Base Spreading Resistance($r_{b'b}$)= h_{ie}-$r_{b'e}$

where h_{ie}=input resistance with output shorted

- The Output Conductance(g_{ce})= h_{oe}-(1+h_{fe}) $g_{b'c}$
  where h_{oe}=conductance with the input open circuited.

Hybrid -pi capacitance:

- There are basically two types of capacitances in pn junction diode i.e. one is junction capacitance and other is diffusion capacitance.
- The active mode BJT has one forward biased pn junction and one reverse biased pn junction. in case of npn BJT the capacitances associated with pn junctions are labeled as:C_{μ}=junction capacitance associate with reversed biased CBJ
  C_{je}= junction capacitance associate with forward biased EBJ
  C_{de}=diffusion capacitance associate with forward biased EBJ
- The diffusion capacitance and junction capacitance associated with forward biased EBJ are appeared parallel and can be combined as

$$C_{\pi} = C_{je} + C_{de} \cong C_{de}$$

- Typically C_{μ} is in the ranges from fraction of pF to few pF where as C_{π} is in the ranges from few pF to tens of pF, which is dominate by C_{de}.

Variation of hybrid-pi parameter:

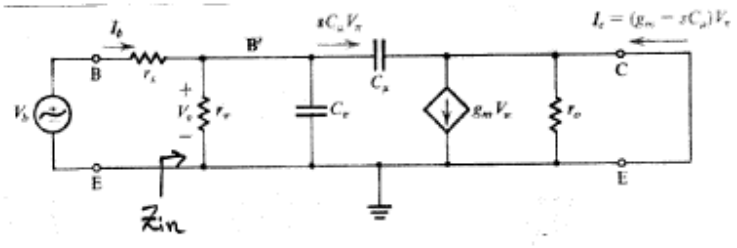
Parameter	Variation with increasing		
	$\|I_C\|$	$\|V_{CE}\|$	T
g_m	Increasing	Independent	Decreasing
$r_{b'b}$	Decreasing		Increasing
$r_{b'e}$	Decreasing	Increasing	Increasing
C_{π}	Increasing	Decreasing	
C_{μ}	Independent	Decreasing	Independent
h_{fe}	Increasing	Increasing	Increasing
h_{ie}	Decreasing	Increasing	Increasing

The CE short-circuits current gain:

an important high frequency characteristics of transistor is unity-gain bandwidth,(f_T). this is defined as the frequency at which short-circuit current gain

$$h_{fe} = {I_c}/{I_b}\Big|_{s.c.load}$$

has decreased to the value one.



The hybrid-pi circuit for a single transistor with short circuit load

Applying KCL at collector terminal provides an equation for short circuit collector current

$$I_c = g_m V_\pi - j\omega C_\mu V_\pi$$

At input terminal B,

$$V_\pi = I_b . Z_{in} = I_b . r_\pi \left(Z_{C_\pi} + Z_{C_\mu}\right)$$

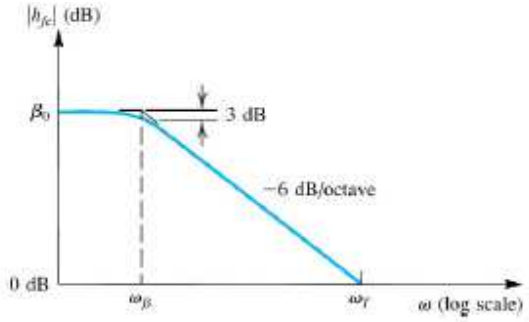
$$V_\pi = I_b . [\frac{1}{r_\pi} + j\omega(C_\pi + C_\mu)]^{-1}$$

$$I_c = (g_m - j\omega C_\mu)\, I_b . [\frac{1}{r_\pi} + j\omega(C_\pi + C_\mu)]^{-1}$$

$$h_{fe} = {I_c}/{I_b} = {(g_m - j\omega C_\mu)}\Big/{[\frac{1}{r_\pi} + j\omega(C_\pi + C_\mu)]}$$

as $g_m \gg |j\omega C_\mu|$ therefore, $h_{fe} \simeq {g_m r_\pi}/{[1 + j\omega(C_\pi + C_\mu) r_\pi]}$

The above frequency response h_{fe} is in the form of single pole low pass circuit.



The short-circuit CE current gain vs. frequency

The 3-db frequency of $|h_{fe}|$is given by

$$\omega_\beta = \frac{1}{(C_\pi + C_\mu) r_\pi} \text{ and } \beta_0 = g_m r_\pi$$

The frequency at which $|h_{fe}|$ declines to value 1 is to denoted as ω_T which can be determine as follows

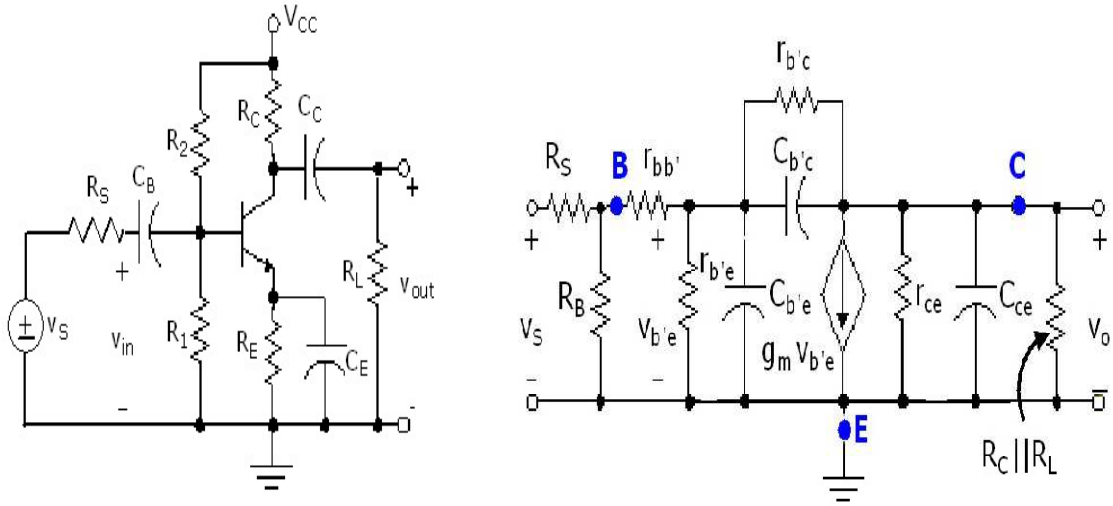
$$|h_{fe}| = 1 = \frac{\beta_0}{[1 + j\omega(C_\pi + C_\mu) r_\pi]}$$

$$\beta_0 = [1 + j\omega(C_\pi + C_\mu) r_\pi] = \left|1 + j\frac{\omega_T}{\omega_\beta}\right|$$

$$\text{For} \omega_T \gg \omega_\beta, \omega_T \simeq {g_m}/{C_\pi + C_\mu}$$

$$f_T \simeq {g_m}/{2\pi(C_\pi + C_\mu)}$$

Common emitter at high frequency:



- all external capacitors are assumed to be short circuits at high frequencies and are not present in the high frequency equivalent circuit (since the external capacitors are large when compared to the internal capacitances, so $Z_c=1/j\omega C$ gets small as the frequency or capacitance gets large).
- simplify the small signal circuit by making the following observations and approximation:
- $C_{ce}$is very small and may be neglected.
- r_{ce}>> $(R_C||R_L)$, r_{ce} so may be neglected since$r_{ce}\|R_C||R_L$ is dominated by $R_C||R_L$.
- $r_{b'c}$ is so much larger than all other resistances that it may be considered "open" and removed from the circuit.
- $r_{bb'} \gg r_{b'c}$so it may be neglected i.e.

$$r_\pi \cong V_{b'e}$$

$$R_{in} = R_B\|r_\pi$$

- The reflection of $C_{b'c}$ to the input and output circuits using Miller's theorem.

CHAPTER-5

(Lecture-15 to 20)

Classification of Amplifiers:

- Classification of amplifier done on the basis of
  I. Frequency range
  II. Method of operation
  III. Ultimate use
  IV. Type of load
  V. Method of interstage coupling
- The frequency classification includes DC (from zero frequency), audio(20Hz to 20KHz), video or pulse(up to few megahertz),radio frequency(a few kilohertz to hundreds of megahertz) and ultrahigh frequency(hundred to thousand megahertz).
- According to the method of operation amplifier are divide into
  I. Class A
  II. Class B
  III. Class AB
  IV. Class C
- The classification according to use includes voltage, power, current or general-purpose amplifier.
- In general, the load of an amplifier is impedance. The two most important special cases are resistive load and the tuned circuit operating near its resonance frequency

Distortion in amplifier:

- The types of distortion that may be exist in amplifier either separately or simultaneously are nonlinear distortion, frequency distortion and delay or phase shift distortion.
- **Nonlinear distortion**: it is due to the production of new frequencies in the output which are not present in the input. This distortion is sometimes referred as “amplitude distortion”.

- **Frequency distortion**: it exists when the signal components of different frequencies are amplified differently. It may be caused by internal devices such as capacitor and coupling circuit.
- **Phase-shift distortion**: it results from unequal phase-shifts of signal of different frequencies.

Frequency response of an amplifier:

- Consider a sinusoidal signal of angular frequency ω represented by $AV_m \sin(\omega t + \varphi)$. If the voltage gain of amplifier has a magnitude A and the signal suffer a phase change θ , then the output will be

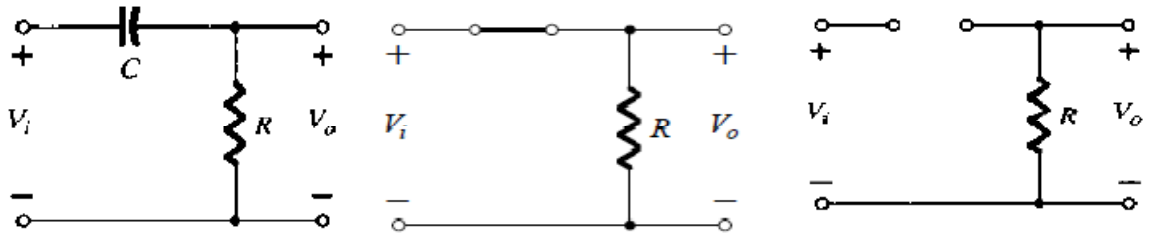
$$AV_m \sin(\omega t + \varphi + \theta) = AV_m \sin[\omega \left(t + \frac{\theta}{\omega}\right) + \varphi]$$

- If the amplification A is independent of frequency and if the phase shift θ is proportional to frequency, then the amplifier will followed the input signal although the signal will be shifted in time by $\frac{\theta}{\omega}$. It means both amplitude and time delay responses are sensitive indicator of frequency distortion.
- For an amplifier stage the frequency characteristic may be divided into three regions.
    i. **Mid-band frequency**: the region of frequency where the amplification and delay is reasonably constant i.e. gain is nearly equal to one.
    ii. **Below mid-band frequency**: in this region, the active circuit may behave as simple high pass circuit. The response decrease with decreasing frequency and output approaches to zero.
    iii. **Above mid-band frequency**: in above mid-band frequency, the circuit behaves like a low pass circuit and the response decreases with increase in frequency.

Low frequency response:

In the low-frequency region of the single-stage BJT or FET amplifier, it is the *R-C* combinations formed by the network capacitors C_c, C_E and C_s and the network resistive parameters that determine the cutoff frequencies. In fact, an *R-C* network similar to the below can be established for each capacitive element and the frequency at which the output voltage drops to 0.707 of its

maximum value determined. Once the cutoff frequencies due to each capacitor are determined, they can be compared to establish which will determine the low-cutoff frequency for the system.



(a) (b) (c)

Fig (a): *R-C* combination that will define a low cutoff frequency

(b): *R-C* circuit at very high frequencies

(c): *R-C* circuit at low frequency i.e. $f = 0$

The output and input voltages are related by the voltage-divider rule in the following manner:

$$V_0 = {RV_i}/{R + X_c}$$

$$A_V = {V_0}/{V_i} = {R}/{(R - jX_c)} = {1}/{1 - j(\frac{X_c}{R})} = {1}/{1 - j(\frac{1}{\omega RC})} = {1}/{1 - j(\frac{1}{2\pi fRC})}$$

$$A_V = \frac{1}{1 - j(\frac{f_1}{f})}$$

Where $f_1 = {1}/{2\pi RC}$

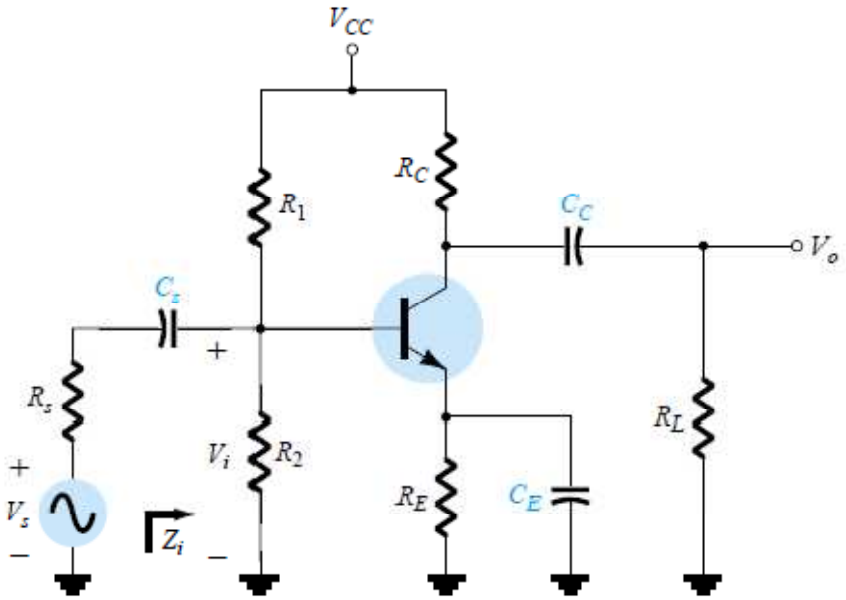
In the magnitude and phase form,

$$A_V = {V_0}/{V_i} = 1 \Big/ \sqrt{1 + \left(\frac{f_1}{f}\right)^2} * \tan^{-1}\left(\frac{f_1}{f}\right)$$

At$f = f_1$,$|A_V| = \frac{1}{\sqrt{2}} = 0.707 \rightarrow -3dB$

Low frequency response of BJT amplifier:

For any BJT configuration, it will simply be necessary to find the appropriate equivalent resistance for the *R-C* combination and the capacitorsC_c, C_E and $C_s$will determine the low-frequency response of the network.



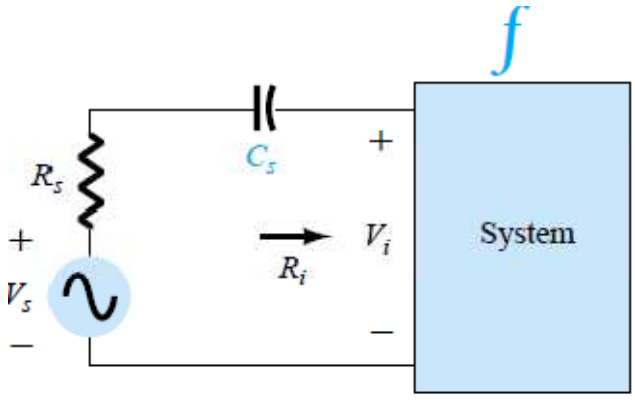
Loaded BJT amplifier with capacitors that affect the low-frequency response

C_s: It is normally connected between the applied source and the active device, the general form of the *R-C* configuration is established by the network. The total resistance is now $R_s + R_i$ and the cutoff frequency is

$$f_{ls} = {}^{1}/_{2\pi(R_s + R_i)C_s}$$

Where R_s= source resistance

R_i= input resistance of the active device



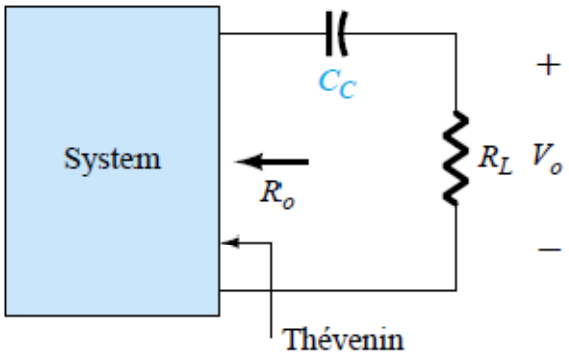
Determining the effect of $C_s$on the low frequency response

C_c: The coupling capacitor is normally connected between the output of the active device and the applied load, the *R-C* configuration that determines the low cutoff frequency due toC_c appears and the total series resistance is now $R_L + R_o$and the cutoff frequency due toC_c is determined by

$$f_{lc} = {}^{1}/_{2\pi(R_o + R_L)C_c}$$

Where R_L= load resistance

R_o=output resistance of active device

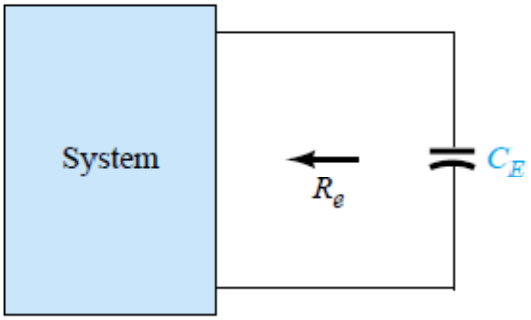


Determining the effect of $C_c$on the low frequency response

C_E: The cutoff frequency due toC_E can be determined using the following equation

$$f_{lc} = {}^{1}/_{2\pi(R_e)C_E}$$

Where R_e=the resistance of active by seen the emitter

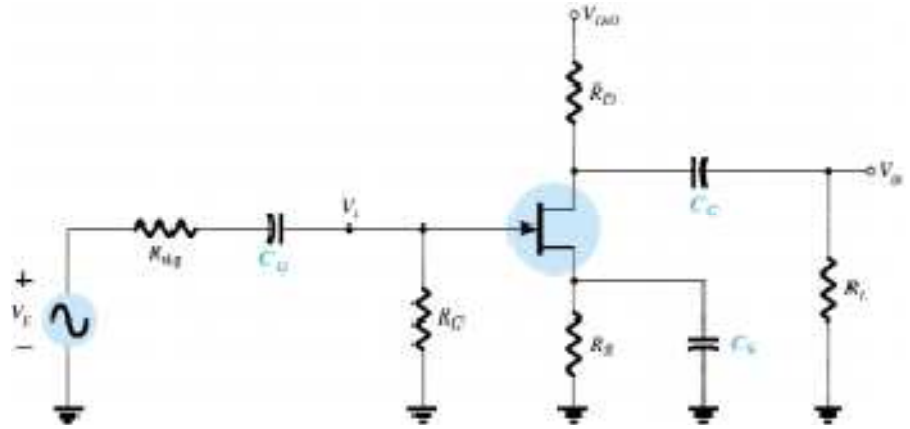


Determining the effect of $C_E$on the low frequency response

The highest low-frequency cutoff determined byC_c, C_E and $C_s$will have the greatest impact since it will be the last encountered before the mid-band level.

Low-frequency response of FET amplifier:

The analysis of the FET amplifier in the low-frequency region will be quite similar to that of the BJT amplifier. There are again three capacitorsC_G, C_c and $C_s$will determine the low-frequency response of the network.



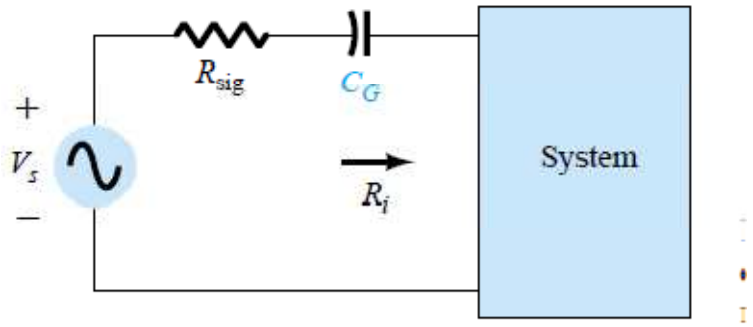
Capacitive elements that affect the low-frequency response of a JFET amplifier

C_G: The coupling capacitor between the source and the active device, the ac equivalent network will appear as shown in below figure. The cutoff frequency determined by $C_G$will then be

$$f_{lG} = {}^{1}/_{2\pi(R_{sig} + R_i)C_G}$$

WhereR_i=input resistance of active device i.e.in FET R_i=R_G

R_{sig}=source resistance



Determining the effect of C_G on the low-frequency response

C_c: The coupling capacitor between the active device and the load the network. The resulting cutoff frequency is

$$f_{lc} = {}^{1}/_{2\pi(R_o + R_L)C_c}$$

WhereR_o=output resistance of active device

R_L =load resistance

Determining the effect of C_c and C_s on the low-frequency response

C_s: It is the source capacitance and the resulting cut off frequency is

$$f_{lc} = {}^{1}/_{2\pi(R_{eq})C_c}$$

Where R_{eq}=$R_S \| \frac{1}{g_m}$ when$r_d \cong \infty$.

High frequency response:

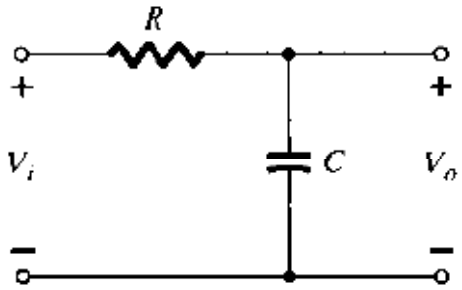
At the high-frequency end, there are two factors that will define the 3-dB point: the network capacitance (parasitic and introduced) and the frequency dependence of$h_{fe}(\beta)$.

In the high-frequency region, the *RC* network of concern has the configuration appearing in the below figure. The gain of the following RC network is given by

$$A_V = \frac{1}{1 + j(\frac{f}{f_2})}$$

Where f_2=cutoff frequency of a device

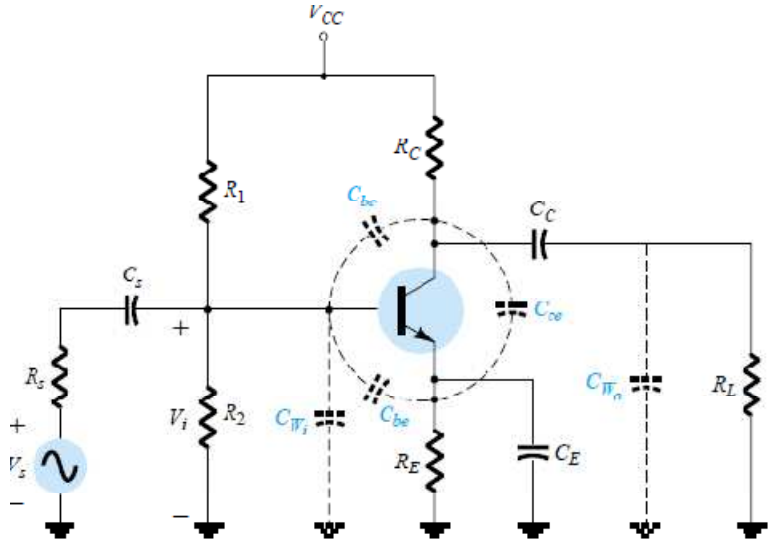
At$f = f_2$,$|A_V| = \frac{1}{\sqrt{2}} = 0.707 \rightarrow -3dB$



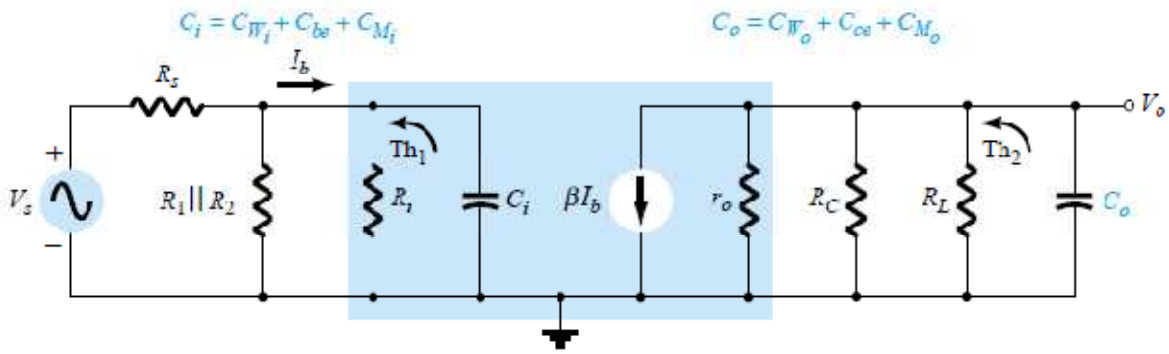
R-C combination that will define a high cutoff frequency

High frequency response of BJT amplifier:

During high frequency response various parasitic capacitances ($C_{be}, C_{ce}\ and\ C_{bc}$) of the transistor have been included with the wiring capacitances (C_{wi}, C_{wo}) introduced in the network. The capacitance $C_i$includes the input wiring capacitanceC_{wi}, the transition capacitanceC_{be}, and the Miller capacitance $C_{M_i}$the capacitance $C_o$includes the output wiring capacitanceC_{wo}, the parasitic capacitanceC_{ce}, and the output Miller capacitanceC_{M_o}. In general, $C_{be}$the capacitance is the largest of the parasitic capacitances, with C_{ce} the smallest. In fact, most significantly the network consists of C_{be}andC_{bc} and do not include C_{ce}unless it will affect the response of a particular type of transistor in a specific area of application.



High-frequency response of BJT amplifier



High-frequency ac equivalent model of BJT amplifier

The Thévenin equivalent circuit for the input and output networks of the above network is given below. For the input network, the3-dB frequency is defined by

$$f_{H_i} = {}^{1}/_{2\pi(R_{Th_1})C_i}$$

Where $R_{Th_1} = R_s \| R_1 \| R_2 \| R_i$

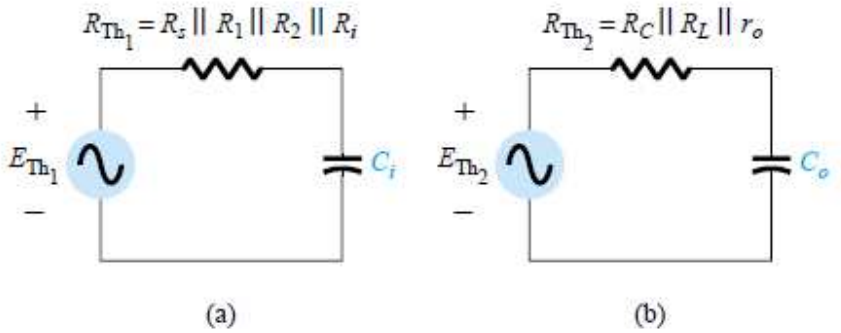
$C_i = C_{M_i} + C_{w_i} + C_{be} = C_{w_i} + C_{be} + (1 - A_v)C_{bc}$

Similarly for output network, the 3-dB frequency is defined by

$$f_{H_o} = {}^{1}/_{2\pi(R_{Th_2})C_o}$$

Where $R_{Th_2} = R_c \| R_L \| r_0$

$C_o = C_{M_o} + C_{w_o} + C_{be}$

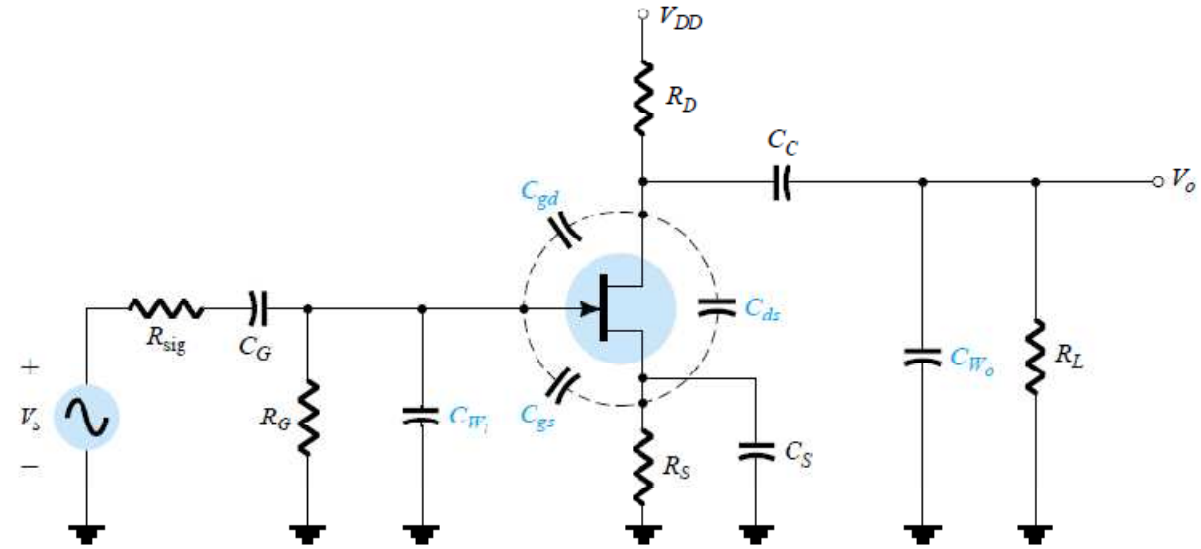


Thévenin circuits for the input and output networks of the network

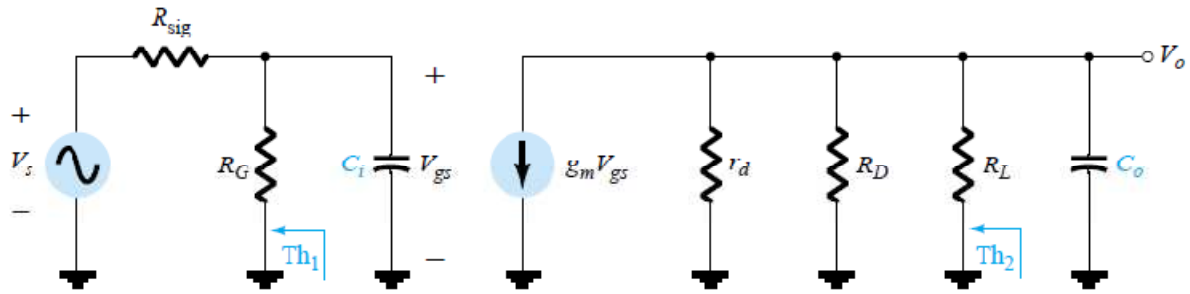
High frequency response of FET amplifier:

The analysis of the high-frequency response of the FET amplifier will proceed in a very similar manner to that encountered for the BJT amplifier. There are interelectrode and wiring capacitances that will determine the high-frequency characteristics of the amplifier. The capacitors C_{gs} and C_{gd} typically vary from 1 to 10 pF, while the capacitance $C_{ds}$is usually quite a bit smaller, ranging from 0.1 to1 pF.

The cutoff frequencies defined by the input and output circuits can be obtained by first finding the Thevenin equivalent circuits for each section.



High-frequency response of FET amplifier



High-frequency ac equivalent model of BJT amplifier

For the input circuit,

$$f_{H_i} = {}^{1}/_{2\pi(R_{Th_1})C_i}$$

Where $R_{Th_1} = R_{sig} \| R_G$

$C_i = C_{M_i} + C_{w_i} + C_{gs} = C_{w_i} + C_{be} + (1 - A_v)C_{gd}$

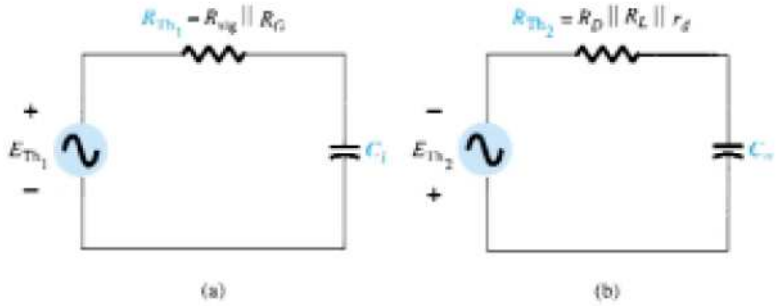
For the output circuit,

$$f_{H_o} = {}^{1}/_{2\pi(R_{Th_2})C_o}$$

Where $R_{Th_2} = R_D \| R_L \| r_d$

$C_o = C_{M_o} + C_{w_o} + C_{ds}$

C_{M_o}=$(1 - {}^{1}/_{A_v})C_{gd}$



The Thevenin equivalent circuits for the (a) input circuit and (b) output circuit

Bode plot:

- Bode plot consists of two plots both have logarithm of frequency on x-axis.
  1. y-axis magnitude of transfer function, H(s), in dB
  2. y-axis phase angle
- The plot can be used to interpret how the input affects the output in both magnitude and phase over frequency.

Procedure to draw magnitude plot in bode plot:
Step1: Determine the Transfer Function of the system

$$H(s) = {K(S + Z_1)}\Big/{S(S + P_1)}$$

Step 2: Rewrite it by factoring both the numerator and denominator into the standard form

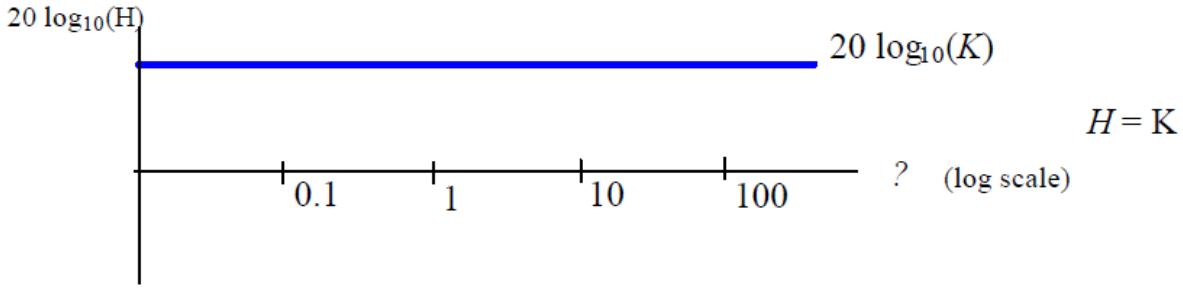
$$H(s) = {KZ_1(\frac{S}{Z_1} + 1)}\Big/{SP_1(\frac{S}{P_1} + 1)}$$

Step 3: Replace ***s*** with ***j?*** Then find the Magnitude of the Transfer Function

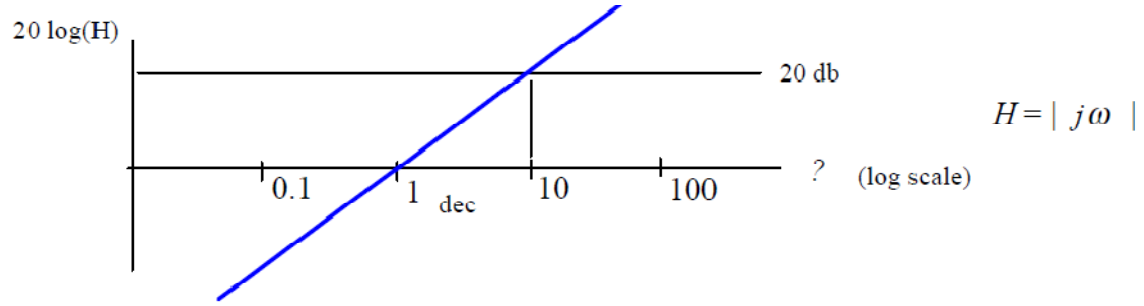
$$H(jw) = {KZ_1(\frac{jw}{Z_1} + 1)}\Big/{jwP_1(\frac{jw}{P_1} + 1)}$$

$$20\log_{10} H(jw) = 20\log_{10} {KZ_1\left(\frac{jw}{Z_1} + 1\right)}\Big/{jwP_1\left(\frac{jw}{P_1} + 1\right)}$$

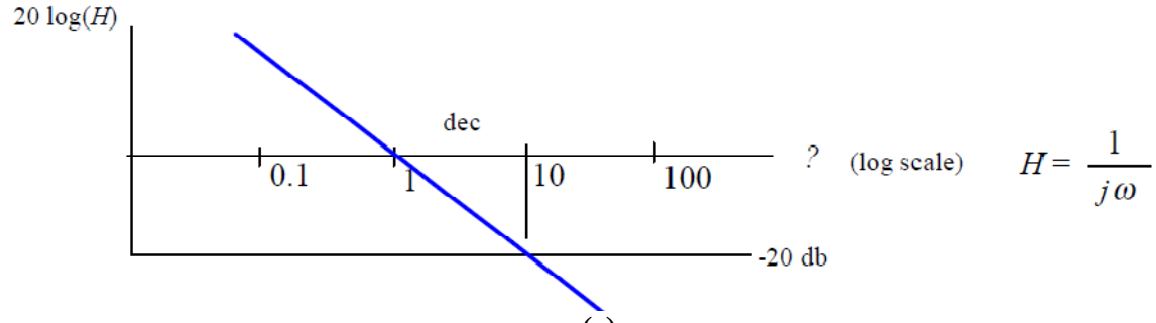
$$= 20\log_{10}|K| + 20\log_{10}|Z_1| + 20\log_{10}\left|\frac{jw}{Z_1} + 1\right| - 20\log_{10}|jw| - 20\log_{10}|P_1|$$
$$+ 20\log_{10}\left|\frac{jw}{P_1} + 1\right|$$



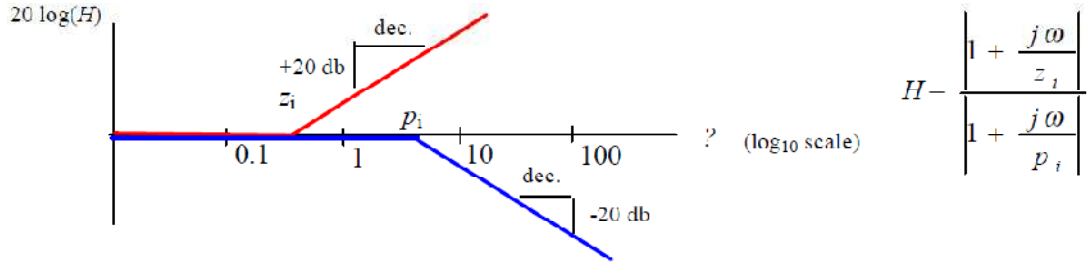
(a)



(b)



(c)



(d)

Figure (a): Effect of constant on magnitude plot.

Figure (b) and (c): Effect of pole and zero at origin on magnitude plot respectively.

Figure (d): Effect of pole and zero not at origin on magnitude plot.

Procedure to draw phase plot in bode plot:

Step 1: the original transfer function

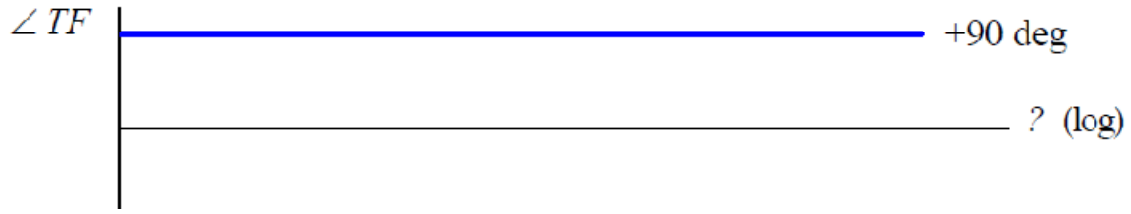
$$H(jw) = \frac{KZ_1(\frac{jw}{Z_1} + 1)}{jwP_1(\frac{jw}{P_1} + 1)}$$

Step 2: the cumulative phase angle associated with this function are given by

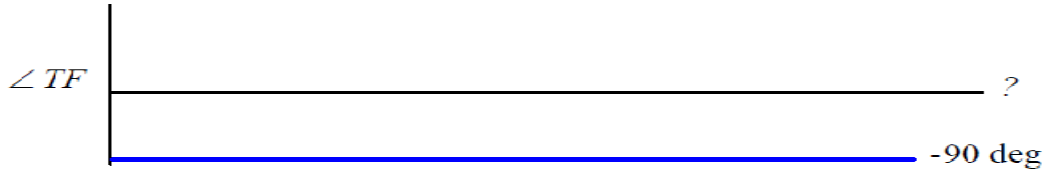
$$\angle H(jw) = \frac{\angle K \angle Z_1 \angle(\frac{jw}{Z_1} + 1)}{\angle jw \angle P_1 \angle(\frac{jw}{P_1} + 1)}$$

Step 3: Then the cumulative phase angle as a function of the input frequency may be written as

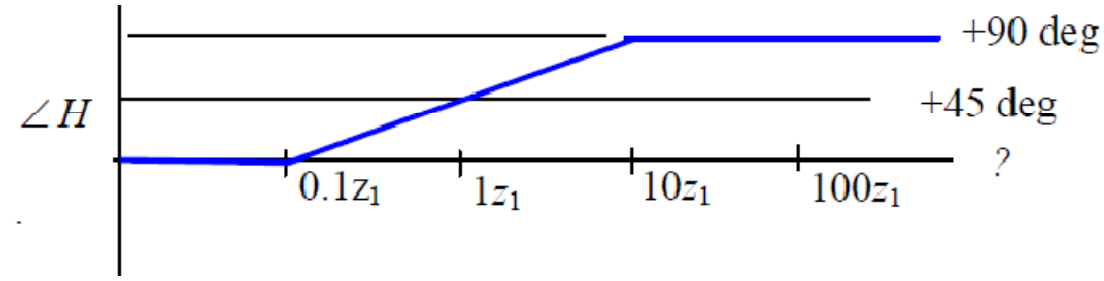
$$\angle H(jw) = \angle(K + Z_1 + \left(\frac{jw}{Z_1} + 1\right) - w - P_1\text{-}(\frac{jw}{P_1} + 1))$$



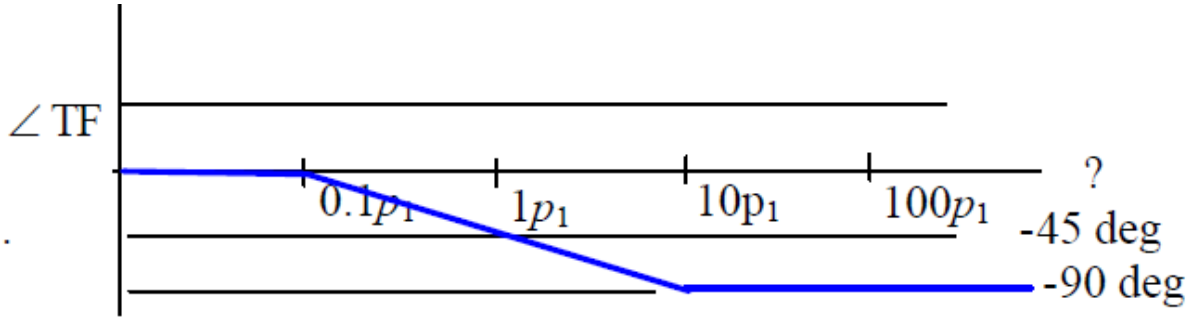
(a)



(b)



(c)



(d)

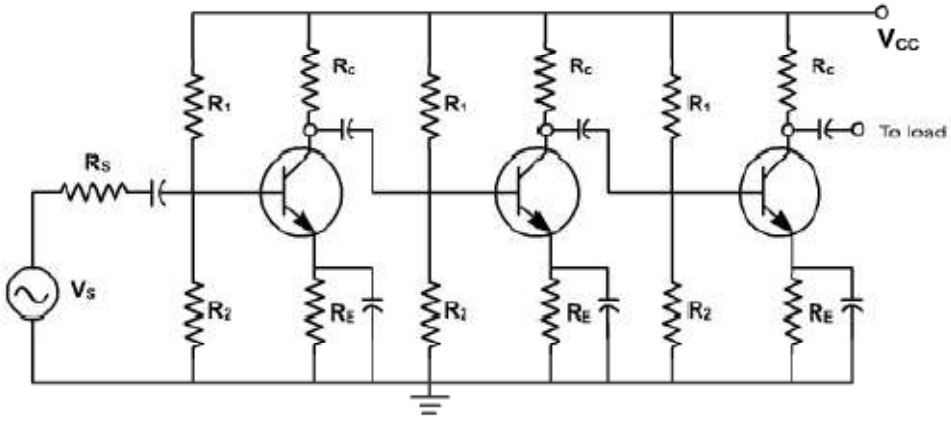
Figure (a): Effect of Zeros at the origin on Phase Angle

Figure (b): Effect of Poles at the origin on Phase Angle

Figure (c): Effect of Zeros not at the origin on Phase Angle

Figure (d): Effect of poles not at the origin on Phase Angle

The RC coupled amplifier:



A cascade common emitter (CE) transistor stage

- It has excellent frequency response in an audio frequency range and cheaper in cost.
- The drawback of this approach is the lower frequency limit imposed by the coupling capacitor and poor impedance matching.