



# VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY : BURLA

(Formerly University College of Engg., Burla-Established by Govt. of Odisha in 1956 & Upgraded in 2009 to A State Govt. University Covered under Section 2(f) & 12(B) of UGC Act.)

P.O: Engineering College, Burla (Siddhi Vihar), Dist: Sambalpur  
Odisha - 768018, INDIA

No. VSSUT/ EE 16576/2016

Dated: 24.05.2016

## ADVERTISEMENT FOR JRF POSITION

Applications are invited for the position of Junior Research Fellow (JRF) funded by SERB, DST in the Electrical Engineering Department under the supervision of Dr. Papia Ray. For details visit the website: [www.vssut.ac.in](http://www.vssut.ac.in).

*Chandrajit*  
24/5/16  
(REGISTRAR)

Memo No. : VSSUT/EE/ 6577 (12)

Date: 24.05.2016

Copy to:

- (1) The Registrar, BPUT, Odisha/ IIT Bhubaneswar/ NIT Rourkela/IIIT Bhubaneswar/Sambalpur University/Utkal University/Berhampur University/Ravenshaw University/ F.M University/OUAT, Bhubaneswar/ G.M. University with a request to display the above advertisement in their notice boards.
- (2) M/S Display line, 219, Sahid Nagar, Bhubaneswar for information with a request to publish the above Advt. in a single issue in daily Odia newspaper "The Samaj" on or before 28/5/2016. Bill in triplicate along with papers in which the Advt. published for necessary Pass & Payment.

*Chandrajit*  
24/5/16  
(REGISTRAR)

Memo No.: VSSUT/EE /6578 (7)

Date: 24.05.2016

Copy to:

1. Dean, Faculty & Planning with a request to hoist the advertisement in the University website [www.vssut.ac.in](http://www.vssut.ac.in) for publicity.
2. University Notice Board/ Dept. Notice Board for affixture
3. PA to Vice-Chancellor for kind information of Hon'ble Vice-Chancellor
4. PA to Registrar for kind information of Registrar.
5. COF, VSSUT, for information and necessary action. This is chargeable to the DST project File No: YSS/2015/001584, Dated. 12.03.2016.
6. Dean, SRIC for kind information and necessary action.
7. HOD, Electrical Engineering for kind information

*Chandrajit*  
24/5/16  
(REGISTRAR)



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No. VSSUT/ EE / 6576/2016

Dated: 24.05.2016

## ADVERTISEMENT FOR JRF POSITION

Applications are invited from highly motivated and eligible candidates for the position of **Junior Research Fellow (JRF)** in **Electrical Engineering** for the following research project funded by Science and Engineering Research Board, Department of Science and Technology, Government of India, under the supervision of Dr. Papia Ray, Assistant Professor, Department of Electrical Engineering, Veer Surendra Sai University of Technology, Odisha.

**Title of the project:** "Assessment of Wide-Area Measurement Signal by Computational Intelligence Techniques".

**Duration of the project:** 3 years

**Name of the position available:** Junior Research Fellow

**Number of position available:** One (01)

**Essential Qualification:**

- (i) M.Tech/M.E degree in Electrical Engineering/Electrical and Electronics Engineering/ or in equivalent streams. A good academic record with a minimum of 60% marks (or 6.5 Grade Point out of 10) in Master's.
- (ii) B.Tech/B.E degree in Electrical Engineering/Electrical and Electronics Engineering/or in equivalent streams with a valid GATE score

**Desirable:** Candidates having exposure to signal processing and machine learning with a good knowledge of programming skills are encouraged to apply

**Fellowship:** As per DST rules- I & II Year-Rs. 25,000/- pm + HRA (if hostel accommodation is not provided), III Year-Rs. 28,000/- pm+ HRA (if hostel accommodation is not provided).

**General terms and conditions:** The position is temporary and renewable each year subject to satisfactory performance for a maximum of three years. The position is coterminous with the project. The candidate selected for this position can also apply for the regular PhD program provided he/she satisfies the existing eligibility criteria for PhD program in the Department of Electrical Engineering, Veer Surendra Sai University of Technology, Odisha.

**How to apply:** Send your curriculum vitae with details of qualifications, experience, latest passport size photo, contact information of at least one referee enclosing self attested copies of marksheet, certificates, publications, testimonials etc and a one page cover letter describing background and motivations to the undersigned by speed post or e-mail. Please write in the subject line/ top of the Envelope- "*Application for the post of Junior Research Fellow*". Interview date will be notified later to the shortlisted candidates only. Please note that no TA/DA will be given to the shortlisted candidates called for the interview.

**Last date for receipt of application:** 28 June 2016

**Dr. Papia Ray (Principal Investigator)**

**Department of Electrical Engineering**

**Veer Surendra Sai University of Technology, Burla, Sambalpur, Odisha, INDIA**

**Pin Code: 768018**

**Mobile: +917749995678 Email: papia\_ray@yahoo.co.in/ raypapia@gmail.com**

**url: <http://www.vssut.ac.in/faculty-profile.php?furl=papia-ray>**