SPONSORSHIP

Prof./Dr./Mr./Ms._____
is an employee of our institute and his/her application is hereby sponsored. The applicant will be permitted to attend the short-term Recent Advancements in Signal Processing, Microwave and VLSI (RASPM-2018) at VSSUT, Burla to be held from 28-05-2018 to 09-06-2018

Signature of sponsoring authority
Date:

Office Seal Designation
DD No:
Date:
Bank:
Amount:

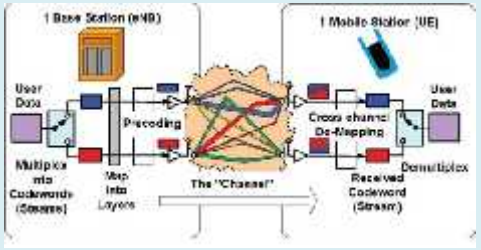
Signature of the applicant

The duly completed application should be mailed to:

Dr. Manoranjan Pradhan/
Dr. NilamaniBhoi / Dr. Ashish Kumar Sharma
Department of Electronics and Telecommunication Engineering,
Veer SurendraSai University of Technology,
Burla, Sambalpur–768018, Odisha, India
Mobile: 9438732346, 8895094663
Email:nilamanib@gmail.com,
aksharma_etc@vssut.ac.in

ABOUT US

Established on 12th Aug. 1956, at Burla in the name of University College of Engineering (UCE), the first engineering college was functioning as a constituent college of Utkal University, Bhubaneswar. The Veer Surendra Sai University of Technology (VSSUT) Odisha was formed by converting UCE to a non-affiliating Unitary University and came into force in the year 2009 by issue of notification by the Industries Department, Government of Odisha. The University occupies nearly 300 acres of prime land in Burla. With a glorious history stretching back over 61 years, providing technical education within a modern educational environment and strong academic staff, VSSUT is identified with engineering education in India. The University has a strong alumni base, most of them occupying coveted positions in many educational, industrial and research organizations all over the world.



Electronics and Telecommunication Engineering Department of VSSUT, BURLA offers an up-to-date 4 year B.Tech Degree course, 2 year M.Tech Degree course in Communication System Engineering, VLSI and Microwave Engineering and PhD in different specializations.

AICTE QIP
Short Term Course
on
Recent Advancements in Signal Processing, Microwave and VLSI (RASPM-2018)
28.05.2018 to 09.06.2018

Coordinators

Dr. Manoranjan Pradhan
Dr. NilamaniBhoi
Dr. Ashish Kumar Sharma

Organized by

Department of Electronics and Telecommunication Engineering
Veer SurendraSai University of Technology, Burla.

OBJECTIVE

This course is conversant with recent advancements in signal processing, microwave and VLSI related algorithms and architectures, which are significant for VLSI based signal processing and microwave communication researchers to use their expertise in the rapid development of wireless communication systems and address the key challenges. The short term course is mainly focused on essential emerging RF & signal wave-front fields for VLSI designing. This short term course RASPM-2018 will bring together signal processing, microwave and VLSI to research community to disseminate new developments and advances in electronics and communication engineering.

COURSE CONTENTS

- Adaptive Computing Using Evolutionary Computing
- Adaptive Signal Processing for modern communication
- Radar Signal Processing
- Modern VLSI & Embedded Systems Opportunistic Spectrum Sensing
- VLSI Design & Semiconductor Devices
- Mixed Mode Analog Circuit Design
- Modern Trends in Antenna design
- MEMS Switches for RF application
- Reconfigurable Antennas
- Fractal Antennas
- Modern Trends in Meta-materials

REGISTRATION DETAILS

No course fees charged for participants sponsored by AICTE approved institutions. However, a caution deposit of Rs.1000/- has to be paid, which will be returned when the participant joins for the course. All payments are to be made in the form of demand draft drawn on any Nationalized Bank and in favor of “Coordinator AICTE QIP STC on RASPM” payable at Burla. Selection will be on first come first served basis and the number of participants is limited to 30. Interested candidates may send an advance copy of the completed application by email to avoid procedural/postal delay.

FINANCIAL ASSISTANCE

Limited number of participants from the AICTE approved institutions will be entitled up to III-AC to and fro railway fare* (via shortest route from the place of work).

*Tatkal charges will not be reimbursed.

FACILITIES

Boarding and lodging facilitieswill be provided for all the outside participants from AICTE approved institutions in the University guest house at Burla in twin sharing basis.

ELIGIBILITY

The course is open to all teachers of degree level AICTE recognized technical Colleges/Universities/ Institutions.

Registration Form

AICTE Sponsored Short Term Course under QIP Scheme on Recent Advancements in Signal Processing, Microwave and VLSI (RASPM-2018)(28.05.2018 to 09.06.2018)

1. Name (Block Letters):
2. Designation &Dept:
3. Organization:
4. Address for communication:

Pin code:

Ph. No.:

E-mail:

5. Highest Academic Qualification:
6. Years of Experience:
7. Specialization:

Only for outside participants:

Draft No.-------- Bank ----------

This is certified that the above information furnished by me is correct to the best of my knowledge and belief.

Date: Signature of the applicant

Important dates:

Last date of receiving applications :25-04-2018

List of shortlisted participants :27-04-2018 (intimated through mail)