



VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY, BURLA
(Formerly University College of Engineering, Burla-Established by Govt. of Odisha in 1956 &
Upgraded in 2009 to A State Govt. University covered under Section 2 (f) & 12 (B) of UGC Act)
P.O: Engineering College, Siddhi Vihar, Burla, Dist: Sambalpur, Odisha – 768 018, India

No. VSSUT/PGSR/ 329 /19

Dated: 13 /06/19

NOTIFICATION

THE DEGREE OF DOCTOR OF PHILOSOPHY IN ENGINEERING

Mr. Bidyadhar Rout, Regd. No. 11060005 is declared to be qualified for the award of the Ph.D Degree in Engineering (**Electrical Engineering**) with effective from **13.06.2019**. The title of the thesis is **“IMPROVEMENT OF POWER SYSTEM STABILITY USING COORDINATED DESIGN OF FACTS DEVICES AND EXCITATION CONTROLLERS”**.

YEAR OF EXAMINATION – 2019

REGISTRATION NO. 11060005

By order of Vice-Chancellor

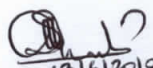
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1. Mr. Bidyadhar Rout, S/o Surendra Kumar Rout, At/Po- Baralpokhri, Via-Charampa, Dist-Bhadrak. (Odisha)-756101.
2. Prof. B B Pati, Professor of Electrical Engineering, VSSUT, Burla – Supervisor
3. Prof. Dinesh Birla, Professor, Department of Electrical Engineering, Rajasthan Technical University, Rawatbhat Road, Kota, Rajasthan (India)-324010 External Examiner of Ph.D Open Viva-voce.
4. Prof. K. A. Folly, Department of Electrical Engineering. University of Cape Town, South Africa- (External Examiner Foreign).
5. All DRC Members.
6. HOD & Chairman, DRC (of Mr. Bidyadhar Rout), Department of Electrical Engineering, VSSUT, Burla for information.
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21. PA to VC for kind information of the Hon'ble Vice-Chancellor.


13/6/2019
Dean, PGS & R