M.Tech-1(PECD/C&I)

ADSP

ADVANCED DIGITAL SIGNAL PROCESSING

Answer SIX Questions including Q.No.1 which is compulsory

Symbols used in this question have their usual meaning.

The figures in right-hand margin indicate marks

FM-70

Time:3 Hours

Q.1 (a) Distinguish between the energy signal and the power signal. Give examples. [2X10]

(b) Find the discrete-time signal having the following Fourier transform

$$X(\omega) = \begin{cases} 0, & 0 \le |\omega| \le \omega_0 \\ 1, & \omega_0 < |\omega| \le \pi \end{cases}$$

(c) Distinguish DFT from DTFT.

(d) Given the FIR filter y(n)= x(n) + 5 x(n-1). Find its unit sample response.

(e) What is frequency response? What is the physical significance?

(f) What is the limit cycle? How to avoid this?

(g) How many complex multiplications and additions are required to compute 64 point DFT in FFT?

(h) Show the periodicity property of a twiddle factor.

(i) What is the linear phase characteristic of FIR filter? Suggest one application area.

(j) Why parametric methods are better than nonparametric methods used for power spectrum estimation?

Q.2 (a) Test the following discrete systems as per the given direction. [2+2+6]

i) y(n) = a+x(n), Linearity test (ii) y(n)= 4x(-n^2), Causality test

(b) Test whether the system y(n)=2-x(-n+1) is shift invariant and stable.

(c) The impulse response of a LTI system is h(n)={1,2,1,3}. Find the response of the system if the input is x (n) = {1, 2, 1, 2}. Use overlap and save method.

Q.3(a) Compute the linearly convolved output using DFT from the following data. [5+5]

N=3, x(n)= -1,2,1 and h(n)=1,2,1

(b) Discuss modulation, time reversal and dilation properties of DFT.

Q.4(a) What is windowing technique ? How it is used for design of digital FIR filters ? [4+6]

(b) Find the system function H(z) of the digital Butterworth filter that meets the following specifications :

(i) 1-dB ripple in the passband $0 \le |\omega| \le 0.3\pi$

(ii) At least 40 dB attenuation in the stop band $0.3\pi \le |\omega| \le \pi$.

Use bilinear transformation method with T=1.

Q.5(a) Draw the flow graph for a 4-point FFT by DFT method. Explain how the same flow graph can be used to compute inverse DFT. [5+5]

(b) Compute the IDFT of the sequence X(k)={3, 2+j, 1, 2-j }.

Q.6(a) Using impulse invariance method obtain the digital transfer function and the Corresponding filter structure [4+4+2]

$H_a(s) = \{1/(s+0.5)(s^2+0.5s+2)\}$. Assume T=1 s.

(b) Draw the corresponding IIR filter structure.

(c) Write two frequency domain properties of IIR filters.

Q.7(a) The input to the system y(n)=0.95 y(n-1) + x(n) is applied through ADC. Assume that the input is quantized to 8 bits. Compute the power produced by the quantization noise. [6+2+2]

(b) What you mean by dynamic range in DSP?

(c) What is a recursive filter? What is coefficient quantization effect in IIR filter?

Q.8 (a)Consider a signal x(n)=s(n)+w(n) , where s(n) is an AR(1) process that satisfies the difference equation s(n)=0.6 s(n-1) + v(n), where {v(n)} is awhite noise sequence with variance σ_v^2=0.64 and {w(n)} is a white noise sequence with variance σ_w^2=1. The processes {v(n)}and {w(n)}are uncorrelated. Designan optimum IIR Wiener filter of length M=2 to estimate {s(n)}. [5+5]

(b) Consider the linear system described by the difference equation

y(n)=0.8 y(n-1) + x(n) + x(n-1), where x(n) is a wide-sense stationary process with zero mean and autocorrelation $\gamma_{xx}(m)=(1/2)^{|m|}$.

(i) Determine the autocorrelation $\gamma_{yy}(m)$ of the output. .

(ii) Determine the power density spectrum of the output {y(n)}.

Total Pages—5

(Set-Q_1)

B.Tech-5th(EE/EEE)
Digital Circuits and Design

Full Marks : 70

Time : 3 hours

Answer **Q.No.1** and any **five** from **Q.No.2** to **Q.No.8**

The figures in the right-hand margin indicate marks

1. Answer the following questions : 2×10

   (*a*) The equivalent number of 13 in radix r is $(23)_r$. Determine r.

   (*b*) An integer represented by sign and 2' complement method is (111010). Represent the same number by 4-bit and 8-bit number system.

   (*c*) Show that the dual of the Exclusive-OR is equal to its complement.

   (*d*) Find the syntax errors in the following declaration and make the corrections :
   module Exmpl-3 (*A*, *B*, *C*, *D*, *F*).

(*e*) Design a combinational circuit with three inputs and one output. The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise. $f = \bar{A}(\bar{B}+\bar{C})$

(*f*) A PN flip-flop has four operations : clear to 0, no change, complement, and set to 1, when Inputs *P* and *N* are 00, 01, 10, 11, respectively. Derive the characteristic equation. $Q_{n+1} = \bar{Q}P + QN$

(*g*) Write the HDL behavioral description of a 4-bit shift register.

(*h*) A 16 K × 4 memory uses coincident decoding by splitting the internal decoder into *X*-selection and *Y*-selection. What is the size of each decoder and how may AND gates are required for decoding the address ? $2^{14} \times 2^{10} = 2^{14}$

(*i*) What is the value of E in following HDL block assuming RA = 1 ?

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RA = RA – 1 ;
if (RA = = 0) E = 1 ;
else E = 0 ;
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(*j*) Calculate the noise margin of the ECL gate, 0.3 volt

2. (*a*) Add the following pair of 6-bit signed two's complement numbers and indicate the overflow if occurs : (*i*) 101110 + 110010; (*ii*) 010101 + 001011. Also obtain the result of two 5-bit two's complement numbers : 01011 * 10101. 5

(*b*) State the overflow rules for subtraction of two's complement signed numbers. Also state the rules of addition of two BCD digits represented by 8-4-2-1 code. 5

3. (*a*) Develop a JK clocked flip-flop using NAND gates only. Tabulate both truth and excitation tables. 4

(*b*) Find the minimal sum-of-product expression for the logic function :

$$F = \sum_{v,w,x,y,z}(5,7,13,15,16,20,25,27,29,31).$$

Realize the function by NAND gates only. 6

4. (*a*) Design a 10-to-4 encoder with inputs 1-out-of-10 code and outputs in BCD in Gray code format. 5

(*b*) Develop a 16-to-1 multiplexer by using 4-to-1 standard iterative multiplexer circuit. 5

5. (*a*) Design a divide by 105 ripple counter by using the circuit with two-feedbacks. 5

(*b*) Using VHDL, design a binary down counter that counts 7 to 0. 5

6. (*a*) Draw a complete logic diagram for a ROM-based circuit that performs combinational multiplication of a pair of 2-bit unsigned integers. 5

(*b*) Design and implement a 2-bit digital comparator. 5

7. (*a*) A clocked synchronous sequential circuit using positive edge-triggered D flip-flops has an input X and an output Y. The excitation equations are :

$D_1 = Q_1 . \overline{X} + \overline{Q_1} . Q_0 . X + Q_1 . \overline{Q_0} . X$

$D_0 = Q_0 . \overline{X} + \overline{Q_0} . X$

and the output equation is $Y = Q_1 . Q_0 . X$. Draw its circuit diagram and obtain its state diagram. 7

(*b*) Explain the following with examples : 3

(*i*) State assignment

(*ii*) State reduction and

(*iii*) equivalent states.

8. (*a*) Determine the high-level output of the RTL gate for a fan-out of 5. Determine also the minimum input voltage required to drive an RTL transistor to saturation when $h_{FE} = 20$. From the above results, determine the noise margin of the RTL gate when the input is high and the fan-out is 5. 6

(*b*) Show the circuit diagram of a four-input NOR gate using CMOS transistors and explain. 4
